DQP-1100
DRV11-WA Compatible Option Module
for NuVAX and NuPDPq
Owner's Manual

DQP-1100-OM
Revision B

Logical®

Owner's Manual for the

DQP-1100

DRV11-WA Compatible Option Module for NuVAX and NuPDPq

Logical®

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Revision B, May 2009

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1 Installation

This chapter lists the steps involved in installing the DQP-1100 option module. The DQP-1100 module is shown in Figure 1-1. Refer to this figure as you follow the steps outlined below.

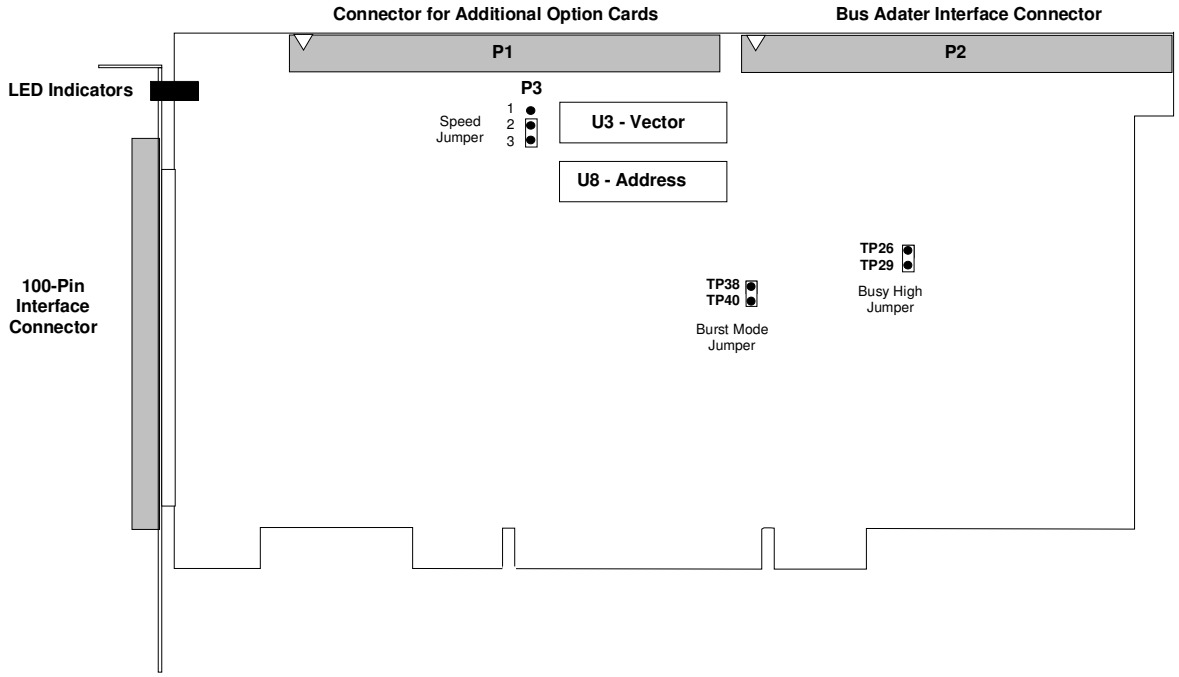


Figure 1-1: DQP-1100 Module

1. Set the switches on the DQP-1100 controller

The DQP-1100 contains two ten-pin DIP switch-packs that allow the user to select device addresses, interrupt vectors, 18 or 22-bit addressing mode, and DRV11-WA or DRV11-B mode.

Note

The DQP-1100 is designed to be compatible with the DRV11-B. However, under VMS, the DQP-1100 is treated as much as possible, like a DRV11-W. Therefore, in order for the device to autoconfigure correctly, you must set the device address and interrupt vector address to those reserved for the DRV11-W.

Mode and Addressing Selection

Use positions 9 and 10 of switch-pack U3 to select operating and addressing modes as shown in Figure 1-2.

Switch position 9	Sets the operating mode to DRV11-WA or DRV11-B. DRV11-WA mode is the standard factory setting
Switch position 10	Sets 18-bit or 22-bit addressing. Note that 18-bit addressing mode should only be used with NuPDP emulating a PDP-11/23.

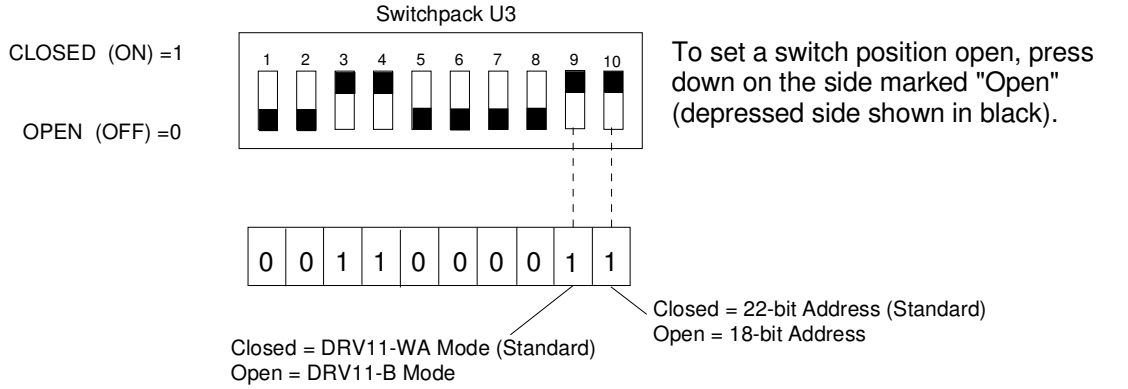


Figure 1-2: Mode and Addressing Switch Settings

Device Address Selection

Use switch-pack U8 to select the device address for the DQP-1100 as shown in Figure 1-3. For the standard address of 17760240, switch positions 1, 2, 3, 4, 5, 7, 9, and 10 are set open; switch positions 6 and 8 are set closed. For DRV11-B emulation, use address 772410.

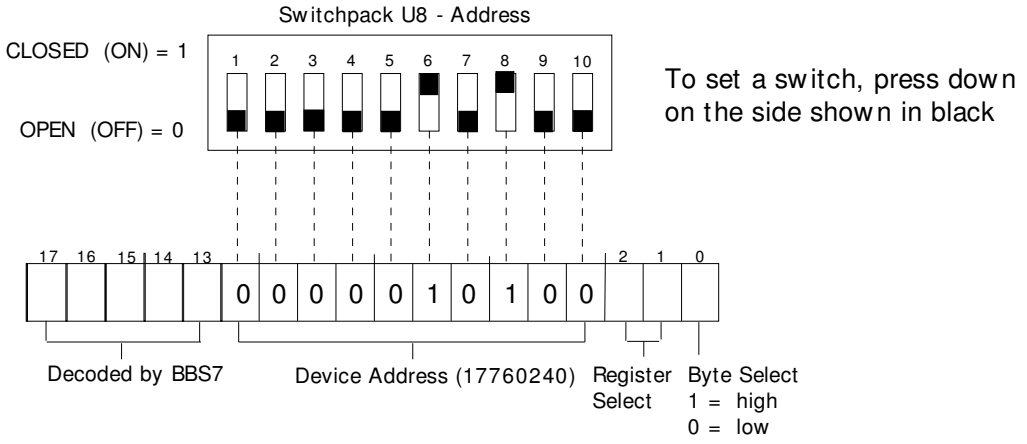


Figure 1-3: Device Address Switch Settings

Interrupt Vector Address Selection

Use switch-pack U3 to select the interrupt vector address for the DQP-1100 as shown in Figure 1-4. For the standard vector of 300, switch positions 1, 2, 5, 6, 7, and 8 are set open; positions 3, 4, 9, and 10 are set closed. For DRV11-B mode, use vector 0124_8.

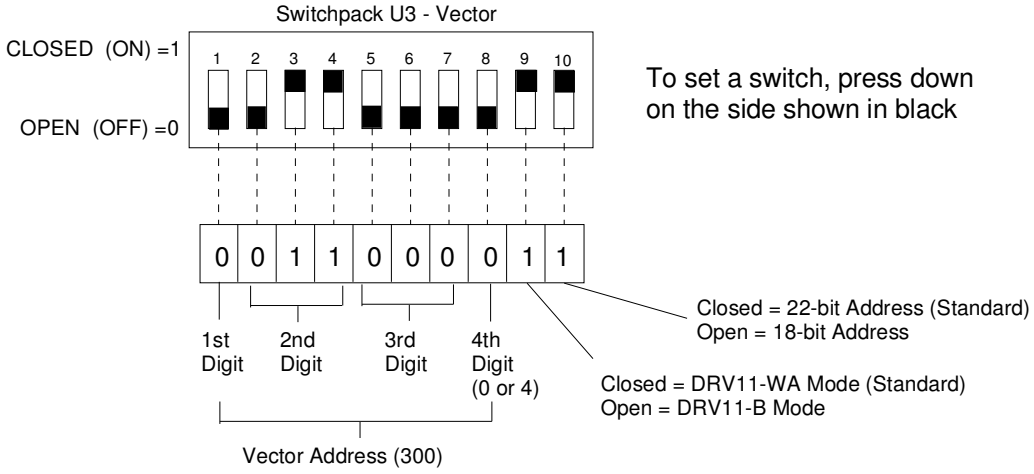


Figure 1-4: Vector Address Switch Settings

2. Configure the DQP-1100 jumpers

The DQP-1100 contains jumpers for selection of burst mode, speed, and busy polarity.

Qbus Burst Mode Jumper

The DQP-1100 is factory set to relinquish Qbus mastership after every eight DMA transfers. The user may select continuous Burst Mode transfers by removing the jumper between TP38 and TP40. When continuous burst mode is selected, the DQP-1100 will relinquish the bus when the CPU or DMA device requests the Qbus, otherwise, the DQP-1100 will retain mastership until the entire transfer is completed.

TP38 to TP40 Installed = Default
TP38 to TP40 Removed = Qbus Burst Mode

Selectable Qbus Burst Mode is provided to support high speed transfers where the DQP-1100 retains mastership of the Qbus for continuous transfers without re-arbitrating for the use of the Qbus. In Qbus Burst Mode, the DQP-1100 only relinquishes the Qbus whenever another DMA device or CPU requests use of the Qbus. When not in Qbus Burst Mode, the DQP-1100 relinquishes the Qbus after eight transfers or whenever another DMA or CPU requests use of the Qbus. In this mode the DQP-1100 needs to have its DMA request re-arbitrated after each eight transfers.

Speed Jumper

This jumper selection allows the user to slow the transfer from the CPU to the user device. Selecting SLOW when operating in user Burst Mode can prevent data overrun conditions. This feature may be especially beneficial when operating in user Burst Mode (SC low) so the user's equipment is not overrun when outputting data to the user equipment. Output data setup time is longer and BUSY low time is increased as shown in Table 1-1.

P3 jumper between 1 and 2 = SLOW
2 and 3 = FAST (Default)

Condition	Fast Mode	Slow Mode	Description
Output Data Setup time	200ns	400ns	The minimum time when data is valid and BUSY trailing edge
BUSY Low Assertion	300ns	500ns	The minimum time between data transfers in User Burst Mode (SC low). In Single Cycle mode (SC high), time between transfers is determined by input signal CYCRQ.

Table 1-1: Slow and Fast Modes

BUSY Signal Jumper

In the default setting (jumper installed), the BUSY signal is true when asserted low. With the jumper removed between TP26 and TP29, the BUSY signal is true when high.

TP26 to TP29 Installed = Default, BUSY low true
TP26 o TP29 Removed = BUSY high true

3. Open the system enclosure

To open the NuVAX or NuPDPq system enclosure:

A. If the system is running, shut down the system software as described in the system manual.

B. Remove power to the system unit.

C. Open the enclosure by removing two thumb screws and sliding the cover towards the rear and lifting. Replace the two thumb screws into the chassis rear panel.

D. Remove the PCI card retainer rail by first lifting the black release knob and then lifting the rail up and out.

4. Install the DQP-1100 module

The DQP-1100 is installed in an option slot next to the bus adapter or other option module.

A. If the back of the expansion chassis or system unit has a metal cover plate over the opening of the slot you have selected, remove the anchor screw that holds the cover in place then slide the cover out of the slot.

B. Position the DQP-1100 with the gold fingers on the edge of the module next to the PCI connector of the selected slot. Gently rock the module into the PCI connector while you fit the metal bulkhead into the slot opening. Be sure that the connectors are firmly seated.

Note: If the enclosure contains RFI clips along the slot, take care when inserting the module not to push the clips out of alignment.

C. Secure the DQP-1100 using the anchor screw that you removed in Step A. Retain the cover plate for future use.

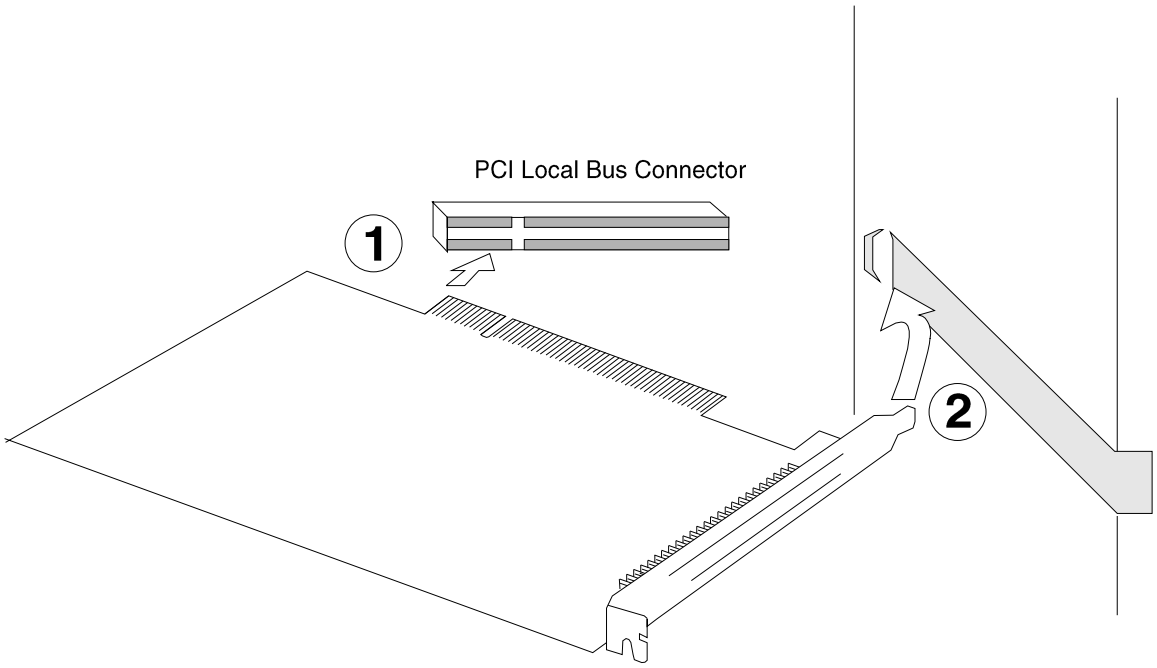


Figure 1-5: Inserting the Board into the PCI Slot

D. Replace the cover on the enclosure and secure.

You are now ready to connect the data cables.

5. Cable the DQP-1100 to the Bus Adapter

Use the supplied CAB-5011-1 cable to connect the first DQP-1100 to the BCI-2300 bus adapter as shown in Figure 1-6. Additional DQP-1100 controllers are added using the CAB-5011-1 as shown in the figure. Align the arrow on the connectors with the red line on the cable.

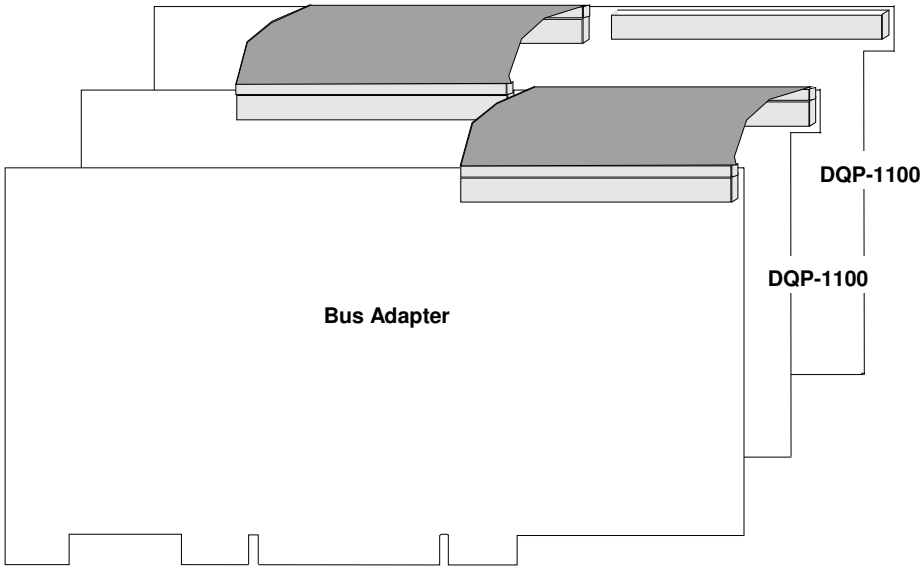
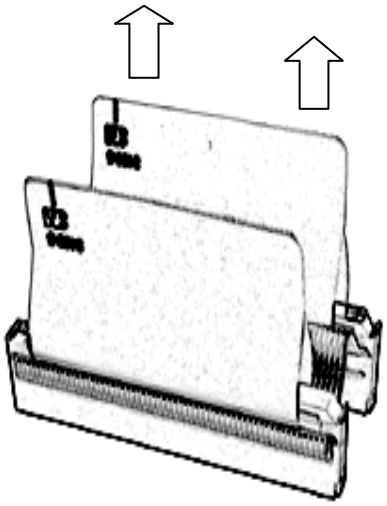


Figure 1-6: Cabling the DQP-1100 and the Bus Adapter

NOTE:
Use care when removing the 60-pin ribbon cable. Use the pull tab and pull the cable straight out from the connector to avoid damage to the connector.



6. Cable the DQP-1100 to the adapter panel

The CPX-1104 adapter panel is shown in Figure 1-7.

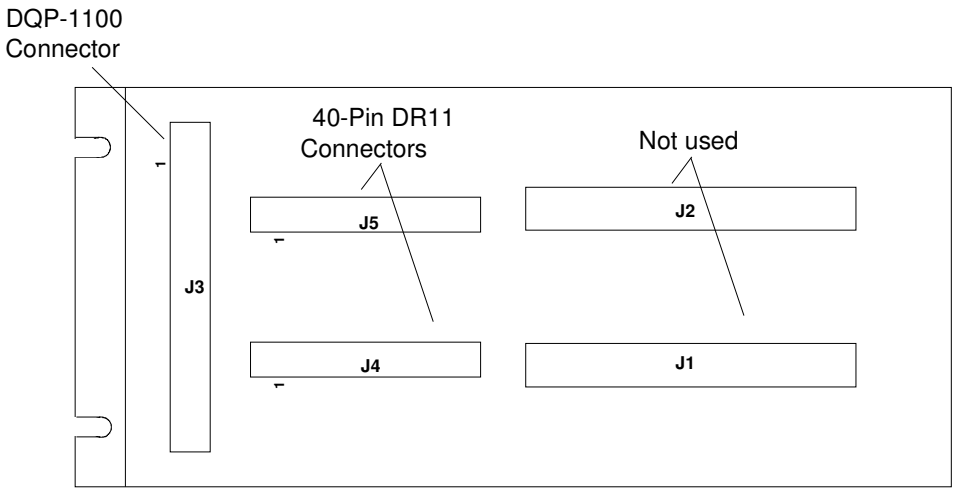


Figure 1-7: CPX-1104 Adapter Panel

Use the supplied 8-foot cable to connect the workstation to the DQP-1100 adapter panel. The adapter panel is provided with screw slots for RETMA rack mount or wall mount. It has no-mar feet for desktop or floor use.

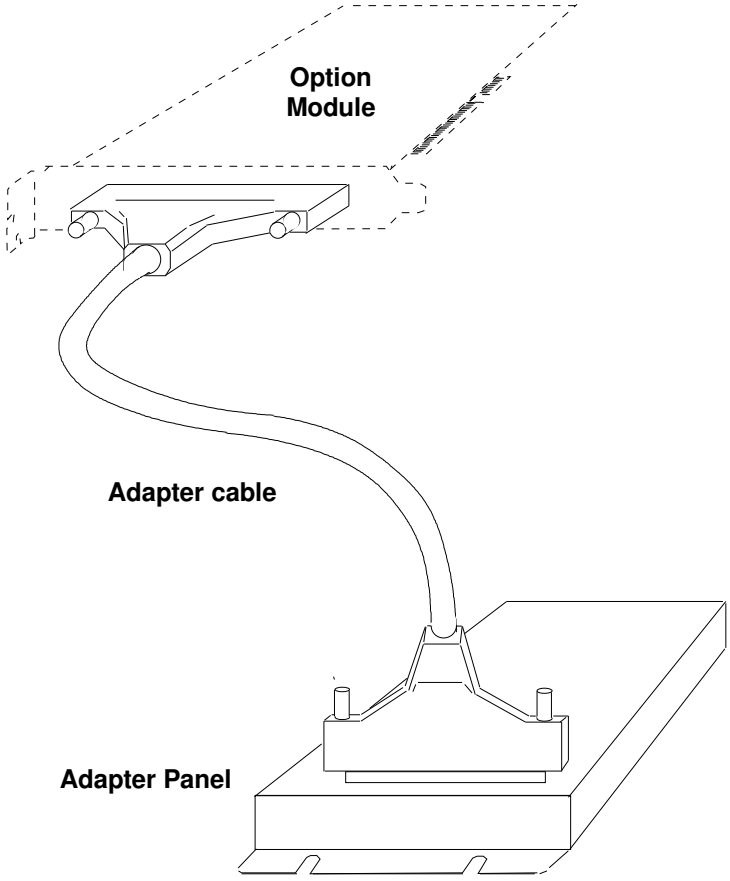


Figure 1-8: Cabling the Option Module to the Adapter Panel

7. Cable the CPX-1104 adapter to user equipment

Use two 40-pin cables to connect the user equipment to the DQP-1100 adapter panel. The function of each interface signal is described in Chapter 2.

J4 and J5 on the CPX-1104 adapter panel correspond to J1 and J2 on Digital's DRV11. Connect user cables to the adapter the same as you would connect to a DRV11. If you are unsure, refer to the connector pin assignments in Appendix B. Be sure to align the triangles on each connector with pin 1.

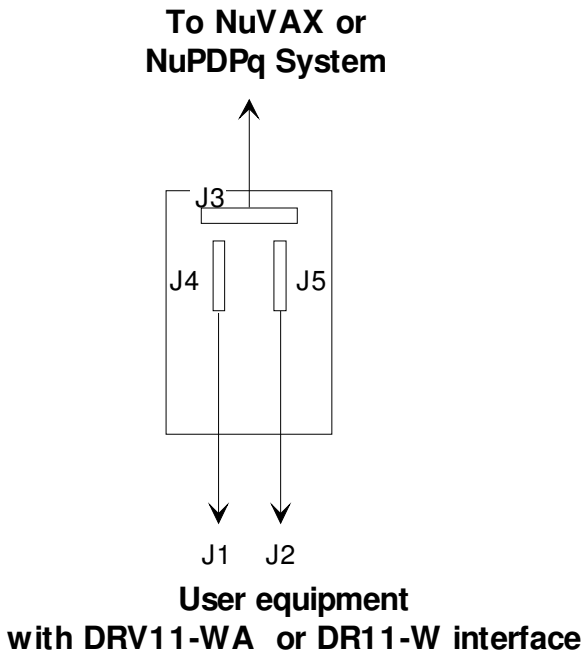


Figure 1-9: Cabling the CPX-1104 Adapter Panel to User Equipment

8. Power up and verify the NuVAX system

This step describes how to verify installation of the DQP-1100 in a NuVAX system. The DQP-1100 is supplied with a CAB-1100-12 loop-back cable to allow you to run Digital's MDM diagnostics as described below. Install CAB-1100-12 between J4 and J5 on the CPX-1104 panel before running diagnostics. Figure 1-7 shows the location of J4 and J5 on the panel.
The following convention is used below:
`user input` In examples, user input is shown in bold type.

Run an individual MDM device test

Using the Webserver, stop the emulator, select the MDM configuration, and restart the emulator.

After about 20 seconds the MDM start-up banner appears and then prompts for the date and time. It is not critical to set the date and time so just press the return key **[cr]**.

Next it will ask for the mode of operation, type: **1 [cr]** to select the 'Menu Mode.'

At the 'Main Menu' type: **4 [cr]** to enter the 'Service Menu.'

At the 'Service Menu' type: **1 [cr]** to enter the 'Set test and message Menu.'

At the 'Set test and message Menu' type: **3 [cr]** to enable 'Stop testing on error.'
Next type **0 [cr]** to return to the 'Service Menu.'

At the 'Service Menu' type: **3 [cr]** to enable the 'Device Menu.'
After all device drivers are loaded enter a **[cr]** and a device list is displayed.

Review the list of devices to determine which you wish to test.
Type the number associated with the device and a return to enter the device test menu.

Type: **2[cr]** to run the device functional tests.
Install a loop-back test cable, if requested, and type [cr] to continue.
After all tests have run or an error occurs, type: 0[cr] to return to the test menu.

Type: **3[cr]** to run the device exerciser test.
Install a loop-back test cable, if requested, and type [cr] to continue.

Allow the device to make 5 passes before stopping.
This exerciser runs until a **Ctrl C** is typed or an error occurs.
Type: **[cr]** to return to the test menu.

Run the MDM System Exerciser

Using the Webserver, stop the emulator, select the MDM configuration, and restart the emulator.

After about 20 seconds the MDM start-up banner appears and then it prompts for the date and time. It is not critical to set the date and time so just press the return key **[cr]**.

Next it will ask for the mode of operation, type: **1 [cr]** to select the 'Menu Mode.'

At the 'Main Menu' type: **4 [cr]** to enter the 'Service Menu.'

At the 'Service Menu' type: **1 [cr]** to enter the 'Set test and message Menu.'

At the 'Set test and message Menu' type: **3 [cr]** to enable 'Stop testing on error.'
Next type **0 [cr]**, to return to the 'Service Menu'.

At the 'Service Menu' type: **3 [cr]** to enable the 'Device Menu.'

After all device drivers are loaded enter a **[cr]** and a device list is displayed.

Review the list of devices to determine which you do not wish to include in the testing.

It is best to disable the testing of **all mass storage devices** preventing the accidental destruction of important files.

Type the number of a device to disable and a return, then type: **1 [cr]** to disable the testing.
Next type **0 [cr]**, to return to the 'Device Menu'.

When you have completed device disabling, type: **0 [cr]** this will return you to the 'Service Menu'.

At the 'Service Menu' type: **2 [cr]** to start the system exerciser. The program will pause and wait for confirmation for any device that requires that a loop-back be installed. Type **[cr]** to confirm the request or type a **Ctrl C** to stop the process and return to the 'Service Menu'. After loop-back confirmation completes, each device will perform a function test and then all devices will have their exercisers started and they will run concurrently until an error is encountered or testing is terminated by typing a **Ctrl C**.

9. Power up and verify the NuPDPq system

This step describes how to verify installation of the DQP-1100 in a NuPDPq system. The DQP-1100 is supplied with a CAB-1100-12 loop-back cable to allow you to run Digital's XXDP diagnostics as described below. Install CAB-1100-12 between J4 and J5 on CPX - 1104 before running the diagnostics. Figure 1-7 shows the location of J4 and J5 on the panel.

The following conventions are used below:

`output` In examples, computer output is shown in this type.

`user input` In examples, user input is shown in bold type.

A. NuPDP is shipped and configured to use a DEC standard, VT100-style terminal and requires CAB-2009-18 or CAB-2010-18 as an adapter cable between the NuPDP serial port and the DEC terminal cable. Terminal emulators or simple character terminals can plug directly into the NuPDP DE9 COM port using a standard cross-over cable and do not require an adapter cable.

B. Open the drive access door and ensure that the system drive cartridge is locked. Keys to the cartridge are supplied with the system.

C. Power up the system. The console displays:

```
Type y to boot XXDP else the OS boots in 4 seconds [Y,N]?Y

BOOTING UP XXDP-XM EXTENDED MONITOR

XXDP-XM EXTENDED MONITOR - XXDP V2.5
REVISION: F0
BOOTED FROM DL0
124KW OF MEMORY
NON-UNIBUS SYSTEM

RESTART ADDRESS: 152000
TYPE "H" FOR HELP !
.
```

D. To run the diagnostic type:

R ZDRVD0 <cr>

The diagnostic begins and displays the following:

ZDRVD0.BIC

Auto Size found DRV11-WA'S at the following locations

DRV11-WA Address = 172410 Vector = 124
MD C-ZDRVD-0 DRV11-WA DMA INTERFACE DIAG

SWR = 000000 NEW =

E. Enter: **100000<cr>**
   If no errors occur the program will start displaying END PASS # messages.

F. Allow a minimum of 10 error free passes.

G. To exit the diagnostic:
   1. Restart the system by pressing the Reset button or cycling power, or
   2. Type CTRL P to display the NuPDP prompt, type HALT to stop the diagnostic. To restart XXDP, type Boot DL0

2 General Description

The DQP-1100 is a direct memory access (DMA) parallel input/output option module which allows real-time collection of parallel data at transfer rates exceeding 4 mbytes/sec of 16-bit words. The DQP-1100 provides access to interface signals on an external cable adapter panel which provides two ports for connection to external devices, an input port and an output port.

Interface Signals

This interface consists of two 40-pin connectors available on the cable adapter panel. Each connector has data signals, control signals, and general purpose signals that permit connecting to another compatible interface.

DRV11, DR11 J1

Signal Name	Signal Description
OUT00 H-OUT15 H	Sixteen data output signals. High true. These signals contain the data last written to the P1DREG register and are normally used as input data to the user equipment.
CYCRQ(A) H	CYCLE REQUEST (A) input signal. High true. A low to high transition initiates a DMA operation when READY is false (Low).
CYCRQB H	CYCLE REQUEST B input signal. This signal is OR'ed with CYCRQ(A) and therefore has an identical function. If this signal is not used, it should be grounded.
ENDCY H	END CYCLE output signal. High true. A 100 ns pulse that indicates the completion of a DR11-W data cycle.
READY H	READY output signal. High true. Set by a PCI Local Bus reset, an ATTN signal received from a user device, or a PCI Local Bus error signal received during a DMA operation. Cleared by writing a one to the GO bit in the Function Output Register (FUNCOREG). When READY is cleared (Low), DMA transfers may be initiated by the user device.

Signal Name	Signal Description
INIT H	INITIALIZE output signal. High true. Set when the PCI Local Bus reset signal is asserted or set by software control via the INIT OUT bit in the Function Output Register (FUNCOREG).
INITV2 H	INITIALIZE V2 output signal. High true. Set when the PCI reset is asserted or when software sets the FNCT2 bit in the Function Output Register (FUNCOREG) a 200ns pulse is generated.
WCINC H	Word Count Increment input signal. Incrementation is always enabled on the DQP-1100 and the state of this signal is ignored.
STATA H	STATUS A input signal. High true. The state of this signal can be read by software via Function Input Register (FUNCIREG) bit 5. When the DQP-1100 is connected to a user device, this signal is user defined. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the FNCT3 signal from the remote controller.
STATB H	STATUS B input signal. High true. The state of this signal can be read by software via Function Input Register (FUNCIREG) bit 4. When the DQP-1100 is connected to a user device, this signal is user defined. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the FNCT2 signal from the remote controller.
STATC H	STATUS C input signal. High true. The state of this signal can be read by software via Function Input Register (FUNCIREG) bit 3. When the DQP-1100 is connected to a user device, this signal is user defined. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the FNCT1 signal from the remote controller.

DRV11, DR11 J2

Signal Name	Signal Description
IN00 H-IN00 H	Sixteen data input signals. High true. These signals contain the data received from the user device when reading the P0DREG register.
ATTN H	ATTENTION input signal. High true. If this signal is driven high by the user device, any transfer between the DQP-1100 and the user device is terminated and the READY signal is asserted. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this signal is controlled by the FNCT2 (INITV2) signal from the remote controller.
BUSY L	BUSY output signal. Low true. The DQP-1100 drives this signal low when internally retrieving data to present to the user device and the signal transitions to high when data is available for the user device; or the DQP-1100 drives this signal low when accepting data from the user device and the signal transitions to high when the user data has been accepted by the DQP-1100. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this signal drives the CYCRQ (A) signal of the remote controller. The polarity of BUSY is controlled by software via the Configuration Register (CONFREG) and can be changed from the standard low true setting to a high true setting.
GO H	GO output signal. High true. When software sets Function Output Register (FUNCOREG) bit 4 to one, a 200ns pulse is generated on the GO output signal and the READY signal is unasserted (Low), allowing transfers to occur between the DQP-1100 and the user device.
C1 H	Control bit 1 input signal. High true. This signal is used to specify the direction that data will move between the DQP-1100 and the user device. When the bit is set high, data is transferred to the DQP-1100 from the user device. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this bit is controlled by the FNCT1 signal from the local controller.
C0 H	Control bit 0 input signal. The DQP-1100 does not support byte DMA transfers, therefore the state of this signal is ignored. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the INIT signal from the remote controller. The state of the signal can be read by software via Function Input Register (FUNCIREG) bit 1.
A0 H	Address bit 0 input signal. The DQP-1100 does not support byte DMA transfers therefore the state of this signal is ignored. When the DQP-1100 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the READY signal from the remote controller. The state of the signal can be read by software via Function Input Register (FUNCIREG) bit 0.
BAINC H	Bus Address Increment input signal. Incrementation is always enabled on the DQP-1100 and the state of this signal is ignored.

Signal Name	Signal Description
FNCT3 H	FUNCTION 3 output signal. High true. The state of this signal is controlled by software via Function Output Register (FUNCOREG) bit 2. When the DQP-1100 is connected to a user device, this signal is user defined. When the DQP-1100 is connected to another DRV11 or DR11 compatible device, this signal controls the state of STATA and SC in the remote controller and when the bit is set to one it specifies single cycle DMA cycles.
FNCT2 H	FUNCTION 2 output signal. High true. The state of this signal is controlled by software via Function Output Register (FUNCOREG) bit 1. When the DQP-1100 is connected to a user device, this signal is user defined. When the DQP-1100 is connected to another DRV11 or DR11 compatible device, this signal controls the state of STATB in the remote controller and when the bit is set to one an INITV2 signal is generated.
FNCT1 H	FUNCTION 1 output signal. High true. The state of this signal is controlled by software via Function Output Register (FUNCOREG) bit 0. When the DQP-1100 is connected to a user device, this signal is user defined. When the DQP-1100 is connected to another DRV11 or DR11 compatible device, this signal controls the state of STATC in the remote controller and the state of C1 in the local controller. When the bit is set to one, the local controller performs DMA write to memory cycles, and when set to zero the local controller performs DMA read from memory cycles.

Specifications

Physical

Controller	Standard short card measuring 6.875 inches by 4.2 inches (17.46 cm by 10.67 cm).

Interface

DQP-1100-A Controller	100-pin high density connector
Adapter Panel (CPX-1104)	Provides user connection to two 40-pin DRV11-WA and DR11-W style connectors
Adapter Cable (CAB-1104-8)	8-foot terminated with 100-pin connectors.

Electrical

Power Required:	
+5 volts DC	0.5 amps
+3.3 volts DC	0.4 amps

PCI Local Bus

Signaling	Universal, +3.3 volt and +5 volt
Addr/Data	32-bit
Clock Rate	33 MHz
Compliance	2.1

Performance

Throughput	Up to 4 Mbytes per second

Environmental

Operating Conditions:

Temperature	5° to 50° C (41° to 122° F)
Relative Humidity	20% to 80% non-condensing

Storage Conditions:

Temperature	-40° to 66° C (-40° to 150° F)
Relative Humidity	10% to 95% non-condensing

Appendix A
PCI Local Bus Interface Connector Pin Assignments

This appendix lists the pin assignments for the PCI bus interface.

Pin	Signal	Pin	Signal
A1	TRST-L	B1	-12V
A2	+12V	B2	TCK-H
A3	TMS-H	B3	GND
A4	TDI-H	B4	TDO-H
A5	+5V	B5	+5V
A6	INTA-L	B6	+5V
A7	INTC-L	B7	INTB-L
A8	+5V	B8	INTD-L
A9		B9	PRSNT1-L
A10	+5V	B10	
A11		B11	PRSNT2-L
A12	GND	B12	GND
A13	GND	B13	GND
A14		B14	
A15	RST-L	B15	GND
A16	+5V	B16	CLK-H
A17	GNT-L	B17	GND
A18	GND	B18	REQ-L
A19		B19	+5V
A20	AD30-H	B20	AD31-H
A21	+3.3V	B21	AD29-H
A22	AD28-H	B22	GND
A23	AD26-H	B23	AD27-H
A24	GND	B24	AD25-H
A25	AD24-H	B25	+3.3V
A26	IDSEL-H	B26	C/BE3-L
A27	+3.3V	B27	AD23-H
A28	AD22-H	B28	GND
A29	AD20-H	B29	AD21-H
A30	GND	B30	AD19-H

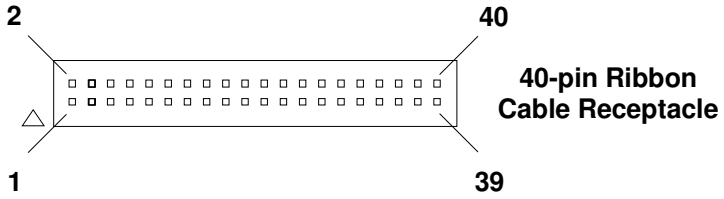
Pin	Signal	Pin	Signal
A31	AD18-H	B31	+3.3V
A32	AD16-H	B32	AD17-H
A33	+3.3V	B33	C/BE2-L
A34	FRAME-L	B34	GND
A35	GND	B35	IRDY-L
A36	TRDY-L	B36	+3.3V
A37	GND	B37	DEVSEL-L
A38	STOP-L	B38	GND
A39	+3.3V	B39	LOCK-L
A40	SDONE-H	B40	PERR-L
A41	SBO-L	B41	+3.3V
A42	GND	B42	SERR-L
A43	PAR-H	B43	+3.3V
A44	AD15-H	B44	C/BE1-L
A45	+3.3V	B45	AD14-H
A46	AD13-H	B46	GND
A47	AD11-H	B47	AD12-H
A48	GND	B48	AD10-H
A49	AD09-H	B49	GND
A50	KEYWAY	B50	KEYWAY
A51	KEYWAY	B51	KEYWAY
A52	C/BE0-L	B52	AD08-H
A53	+3.3V	B53	AD07-H
A54	AD06-H	B54	+3.3V
A55	AD04-H	B55	AD05-H
A56	GND	B56	AD03-H
A57	AD02-H	B57	GND
A58	AD00-H	B58	AD01-H
A59	+5V	B59	+5V
A60	REQ64-L	B60	ACK64-L
A61	+5V	B61	+5V
A62	+5V	B62	+5V

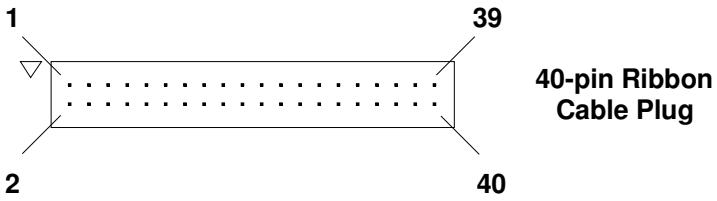
Appendix B
CPX-1104 Adapter Panel Connectors

This appendix lists the pin assignments for the CPX-1104 connectors. The CPX-1104 contains two 40-pin connectors for DRV11-WA and DR11-W interface connection, and a 100-pin SCSI-style receptacle for connection to the DQP-1100 option module.

DRV11-WA and DR11-W Pin Assignments

The connector used for DRV11-WA and DR11-W interfaces is a 40-pin receptacle, 3M part number 2540-6002-UB. It and the mating cable connector are shown below.





Connector J4 (DR11 J1)

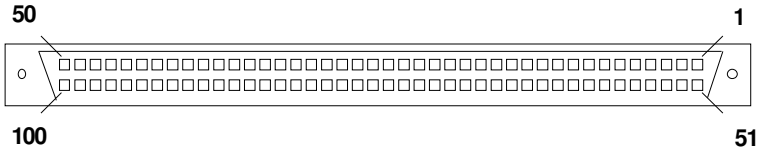
Signal	3M Pin	Berg Pin	Berg Pin	3M Pin	Signal
OUT15 H	1	VV	UU	2	OUT00 H
OUT14 H	3	TT	SS	4	OUT01 H
OUT13 H	5	RR	PP	6	OUT02 H
OUT12 H	7	NN	MM	8	OUT03 H
OUT11 H	9	LL	KK	10	OUT04 H
OUT10 H	11	JJ	HH	12	OUT05 H
OUT09 H	13	FF	EE	14	OUT06 H
OUT08 H	15	DD	CC	16	OUT07 H
GND	17	BB	AA	18	GND
CYCRQB H	19	Z	Y	20	GND
ENDCY H	21	X	W	22	GND
STATC H	23	V	U	24	GND
STATC H	25	T	S	26	GND
STATB H	27	R	P	28	GND
INIT H	29	N	M	30	GND
STATA H	31	L	K	32	SC H,BURST L
WCINC H	33	J	H	34	GND
READY H	35	F	E	36	GND
INITV2 H	37	D	C	38	GND
CYCRQA H	39	B	A	40	GND

Connector J5 (DR11 J2)

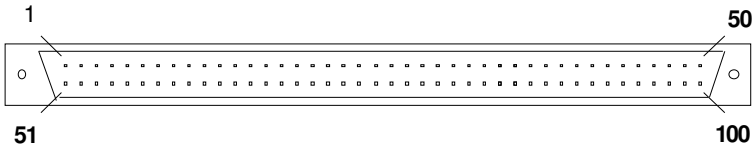
Signal	3M Pin	Berg Pin	Berg Pin	3M Pin	Signal
IN15 H	1	VV	UU	2	IN00 H
IN14 H	3	TT	SS	4	IN01 H
IN13 H	5	RR	PP	6	IN02 H
IN12 H	7	NN	MM	8	IN03 H
IN11 H	9	LL	KK	10	IN04 H
IN10 H	11	JJ	HH	12	IN05 H
IN09 H	13	FF	EE	14	IN06 H
IN08 H	15	DD	CC	16	IN07 H
GND	17	BB	AA	18	GND
GND	19	Z	Y	20	GND
GO H	21	X	W	22	GND
FNCT1 H	23	V	U	24	GND
C1 H	25	T	S	26	GND
FNCT2 H	27	R	P	28	GND
C0 H	29	N	M	30	GND
FNCT3 H	31	L	K	32	FNCT3 H
BAINC H	33	J	H	34	GND
A00 H	35	F	E	36	GND
ATTN H	37	D	C	38	GND
BUSY L,BUSY H	39	B	A	40	GND

DQP-1100 Connector Pin Assignments

The high density connector on the DQP-1100 option module (J1) is AMP part number 749076-9 or Thomas & Betts Ansley part number HFR100RA29BX1. It is a 100-pin SCSI style receptacle. Both it and the mating cable connector are shown below. The pin assignments are listed below.



100-pin High Density Panel Receptacle



100-pin High Density Cable Plug

CPX-1104 Connector J3

Pin	Signal	Signal	Pin
1	IN00 H	OUT00 H	51
2	GND	GND	52
3	IN01 H	OUT01 H	53
4	GND	GND	54
5	IN02 H	OUT02 H	55
6	GND	GND	56
7	IN03 H	OUT03 H	57
8	GND	GND	58
9	IN04 H	OUT04 H	59
10	GND	GND	60
11	IN05 H	OUT05 H	61
12	GND	GND	62
13	IN06 H	OUT06 H	63
14	GND	GND	64
15	IN07 H	OUT07 H	65
16	GND	GND	66
17	IN08 H	OUT08 H	67
18	GND	GND	68
19	IN09 H	OUT09 H	69
20	GND	GND	70
21	IN10 H	OUT10 H	71
22	GND	GND	72
23	IN11 H	OUT11 H	73
24	GND	GND	74
25	IN12 H	OUT12 H	75
26	GND	GND	76
27	IN13 H	OUT13 H	77
28	GND	GND	78
29	IN14 H	OUT14 H	79
30	GND	GND	80
31	IN15 H	OUT15 H	81
32	GND	GND	82
33	ATTN H	INITV2 H	83
34	GND	GND	84
35	BUSY L,BUSY H	CYCRQA H	85
36	GND	GND	86
37	CYCRQB H	+5V	87
38	GND	GND	88
39	C1 H	+5V	89
40	LOOPC1 H	GND	90
41	INIT H	+5V	91
42	GND	GND	92
43	FNCT1 H	STATC H	93
44	A00 H	READY H	94
45	FNCT2 H	STATB H	95
46	C0 H	GO H	96
47	FNCT3 H	STATA H	97
48	SC H,BURST L	ENDCY H	98
49	GND	WCINC H	99
50	BAINC H	GND	100

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