# DQP-1400
# DRV11-J Option Module
## for NuVAX and NuPDPq
## Owner's Manual

**DQP-1400-OM**
**Revision B**

Logical®

# Owner's Manual for the

# DQP-1400

**DRV11-J Compatible Option Module for NuVAX and NuPDPq**

Logical®

Document Number DQP-1400-OM
Revision B, April 2007

# Contents

## Tables

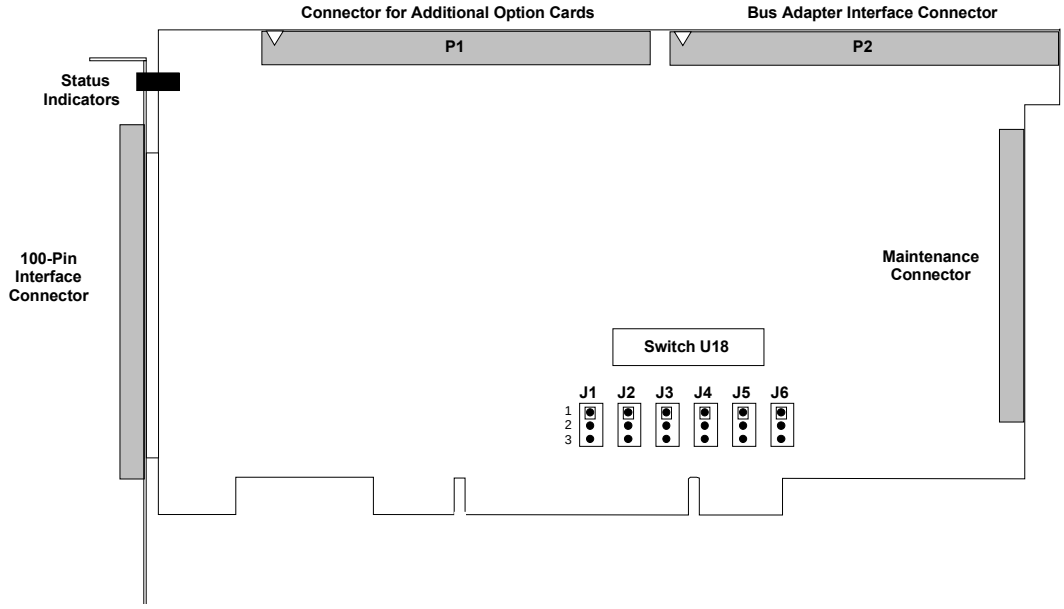


## Illustrations

# 1 Installation

This chapter lists the steps involved in installing the DQP-1400 hardware.

The DQP-1400 module is shown in Figure 1-1. Refer to this figure as you follow the steps outlined below.




**Status Indicators:**
Red indicates that there is a problem with the board.
Green indicates Qbus activity.

Figure 1-1: DQP-1400 Module

# 1. Set the address switch on the DQP-1400

The DQP-1400 contains one ten-pin DIP switch-pack that allows the user to select the device and addresses.

Use the switch-pack at U18 to select the device address for the DQP-1400 as shown in Figure 1-2. For the standard address of 17764160, switch positions 1, 3, 4, 5, 6, and 10 are set open; switch positions 2, 7, 8, and 9 are set closed.

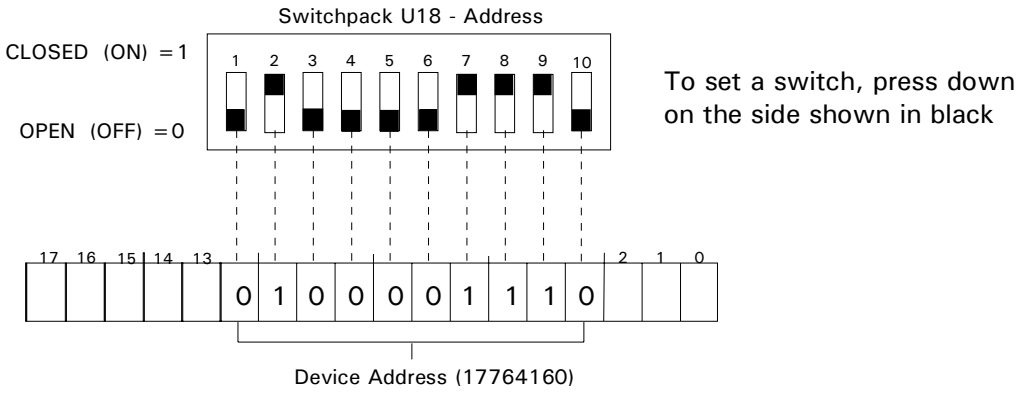



Figure 1-2: Device Address Switch Settings

# 2. Configure the DQP-1400 jumpers

## Interrupt Vector Address Assignment

The DQP-1400 may be programmed to operate in systems that are either interrupt-driven or software-polled. If the DQP-1400 is used in an interrupt-driven system, the interrupt vector addresses must be programmed into a RAM (vector address memory).

A total of 16 vector addresses may be stored in the vector address memory. Although the vector data bits D7 - D0 provide the capability to program addresses in the 0000 through 1774 octal range, (see Figure 1-3), the vector addresses actually assigned must conform to the floating vector conventions established for the Qbus. The floating vector convention used for communications devices (and other devices that interface with the PDP-11 series products) assigns vectors in order, starting at 300 and ending at 776 octal. To avoid device conflicts, refer to the *Microcomputer Interfaces Handbook* when assigning vector addresses.

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | V9 | V8 | V7 | V6 | V5 | V4 | V3 | V2 | 0 | 0 |
| | | | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |

CSRB (Group 1) or CSRD (Group 2)

Figure 1-3: DQP-1400 Vector Address Format

| Jumper | 2 to 3 | 1 to 2 | Description |
|---|---|---|---|
| **Interrupt Selection** | | | |
| J1 | | Installed | Selects the port A high byte signals to be used for generating group 2 vectored interrupts. (Default) |
| | Installed | | Selects port A I/O bits 11-08 and USER RPLY signals A through D. |
| **Priority Selection** | | | |
| J2 | Installed | | BIRQ4 (Default) |
| J3 | Installed | | |
| J2 | | Installed | BIRQ5 |
| J3 | Installed | | |
| J2 | Installed | | BIRQ6 |
| J3 | | Installed | |
| J2 | | Installed | BIRQ7 |
| J3 | | Installed | |
| **Reserved** | | | |
| J4<br>J5<br>J6 | | Installed<br>Installed<br>Installed | Reserved for future use. |

Table 1-1: DQP-1400 Factory Jumper Settings

# 3. Open the system enclosure

To open the NuVAX or NuPDPq system enclosure:

A. If the system is running, shut down the system software as described in the system manual.

B. Remove power to the system unit.

C. Open the enclosure by removing two thumb screws and sliding the cover towards the rear and lifting. Replace the two thumb screws into the chassis rear panel.

D. Remove the PCI card retainer rail by first lifting the black release knob and then lifting the rail up and out.

**Note: Use the anti-static wrist strap supplied with your system unit to prevent damage to the equipment. Clip the free end of the strap to the metal frame of the enclosure.**

# 4. Install the DQP-1400 module

The DQP-1400 is installed in an option slot next to the bus adapter or other option module.

A. If the back of the expansion chassis or system unit has a metal cover plate over the opening of the slot you have selected, remove the anchor screw that holds the cover in place then slide the cover out of the slot.

B. Position the DQP-1400 with the gold fingers on the edge of the module next to the PCI connector of the selected slot. Gently rock the module into the connector while you fit the metal bulkhead into the slot opening. Be sure that the connectors are firmly seated.

**Note: If the enclosure contains RFI clips along the slot, take care when inserting the module not to push the clips out of alignment.**

C. Secure the DQP-1400 using the anchor screw that you removed in Step A. Retain the cover plate for future use.

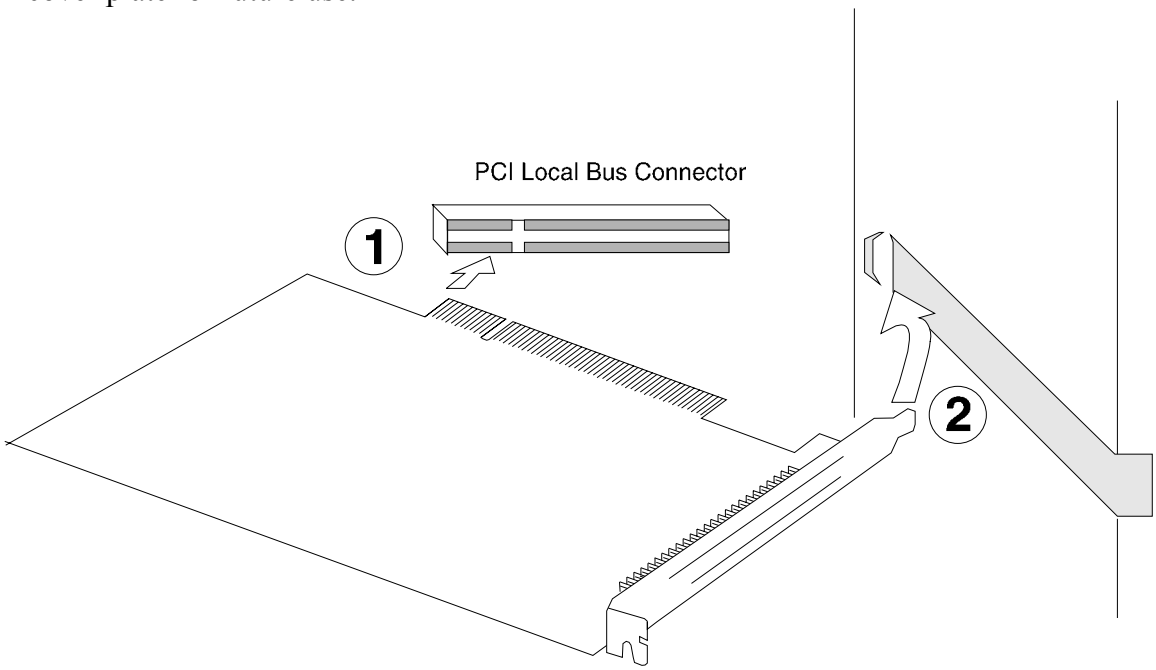



Figure 1-4: Inserting the Board into the Option Slot

D. Remove the anti-static wrist strap, replace the cover on the enclosure and secure.

You are now ready to connect the data cables.

# 5. Cable the DQP-1400 to the bus adapter

Use the supplied CAB-5011-1 cable connect the first option module to the BQP-230x or BPQ-230x bus adapter as shown in Figure 1-5. Additional DQP-1400 controllers are added using the CAB-5011-1 as shown in the figure. Align the arrow on the connectors with the red line on the cable.

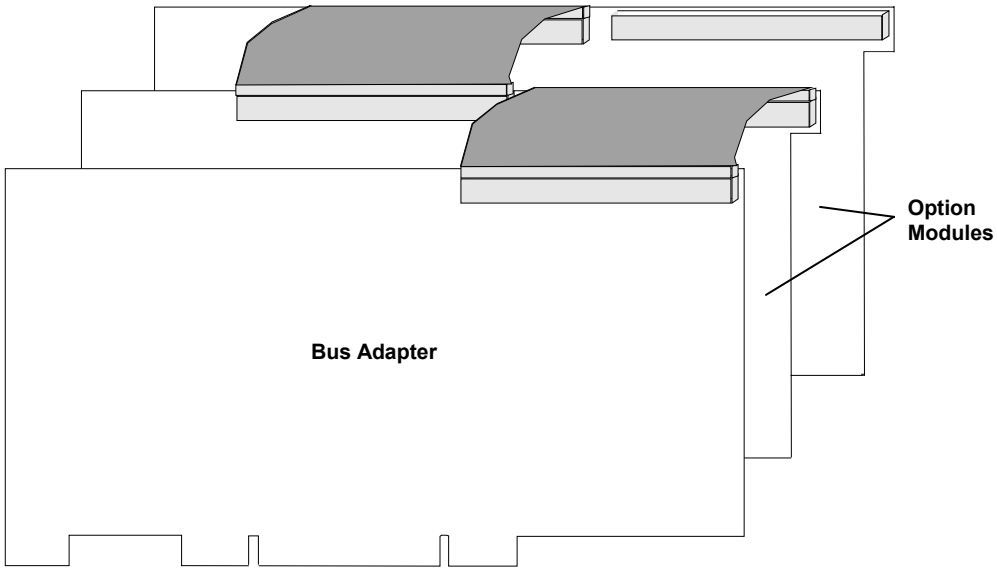
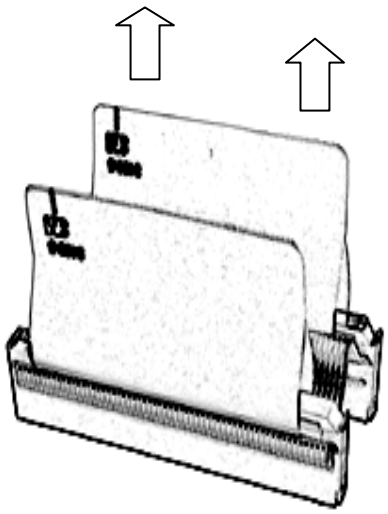



Figure 1-5: Cabling the DQP-1400 and the Bus Adapter

**NOTE:**
Use care when removing the 60-pin ribbon cable. Use the pull tab and pull the cable straight out from the connector to avoid damage to the connector.



# 6. Cable the DQP-1400 to the adapter panel

The CPX-1403 adapter panel is shown in Figure 1-6.

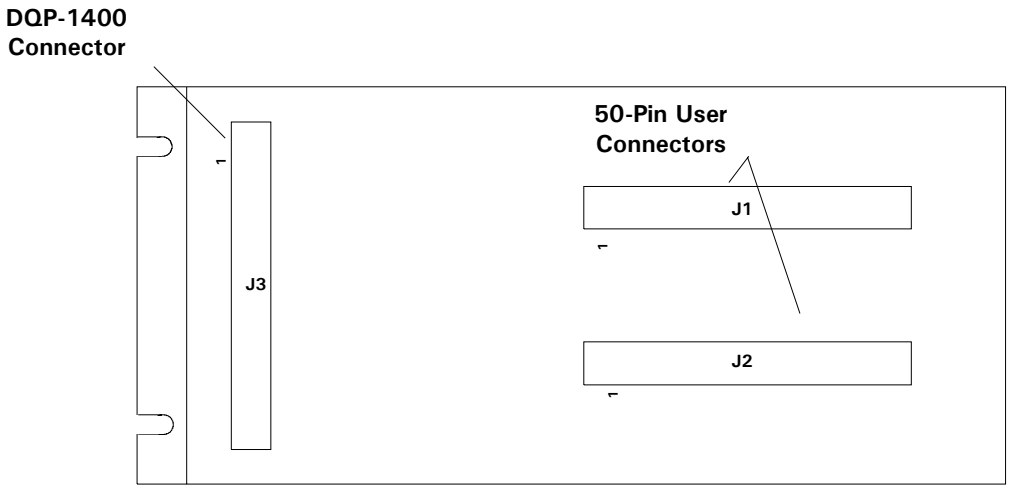



Figure 1-6: CPX-1403 Adapter Panel

Use the supplied 8-foot cable to connect the workstation to the DQP-1400 adapter panel. The adapter panel is provided with screw slots for RETMA rack mount or wall mount. It has no-mar feet for desktop or floor use.

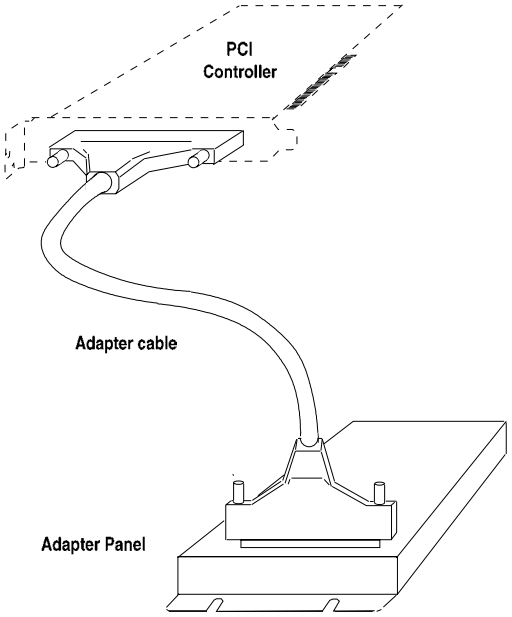



Figure 1-7: Cabling the Controller to the Adapter Panel

# 7. Cable the CPX-1403 adapter to user equipment

Cable the J1 and J2 connectors on the CPX-1403 adapter panel to your DRV11-J compatible user equipment. Align the triangle on the cable connector with the triangle of the panel connector. See Figure 1-6.

Pin assignments for the connectors are listed in Appendix A.

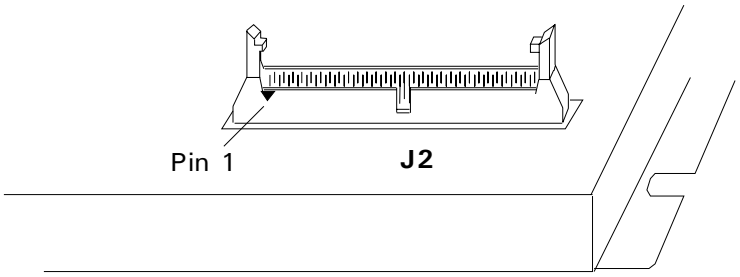



Figure 1-8: CPX-1403 User Connector

# 8. Verify installation in a NuVAX system

**A. Run an individual MDM device test**

Using the Webserver, stop the emulator, select the MDM configuration, and restart the emulator.

After about 20 seconds the MDM start-up banner appears and then prompts for the date and time. It is not critical to set the date and time so just press the return key **[cr]**.

Next it will ask for the mode of operation, type: **1 [cr]** to select the 'Menu Mode.'

At the 'Main Menu' type: **4 [cr]** to enter the 'Service Menu.'

At the 'Service Menu' type: **1 [cr]** to enter the 'Set test and message Menu.'

At the 'Set test and message Menu' type: **3 [cr]** to enable 'Stop testing on error.'
Next type **0 [cr]** to return to the 'Service Menu.'

At the 'Service Menu' type: **3 [cr]** to enable the 'Device Menu.'
After all device drivers are loaded enter a **[cr]** and a device list is displayed.

Review the list of devices to determine which you wish to test.
Type the number associated with the device and a return to enter the device test menu.

Type: **2[cr]** to run the device functional tests.
Install a loop-back test cable, if requested, and type [cr] to continue.
After all tests have run or an error occurs, type: 0[cr] to return to the test menu.

Type: **3[cr]** to run the device exerciser test.
Install a loop-back test cable, if requested, and type [cr] to continue.

Allow all devices to make 10 passes before stopping.
This exerciser runs until a **Ctrl C** is typed or an error occurs.
Type: **[cr]** to return to the test menu.

**B. Run the MDM System Exerciser**

Using the Webserver, stop the emulator, select the MDM configuration, and restart the emulator.

After about 20 seconds the MDM start-up banner appears and then it prompts for the date and time. It is not critical to set the date and time so just press the return key **[cr]**.

Next it will ask for the mode of operation, type: **1 [cr]** to select the 'Menu Mode.'

At the ‘Main Menu’ type: **4 [cr]** to enter the ‘Service Menu.’

At the ‘Service Menu’ type: **1 [cr]** to enter the ‘Set test and message Menu.’

At the ‘Set test and message Menu’ type: **3 [cr]** to enable ‘Stop testing on error.’
Next type **0 [cr]**, to return to the ‘Service Menu’.

At the ‘Service Menu’ type: **3 [cr]** to enable the ‘Device Menu.’

After all device drivers are loaded enter a **[cr]** and a device list is displayed.

Review the list of devices to determine which you do not wish to include in the testing.

It is best to disable the testing of **all mass storage devices** preventing the accidental destruction of important files.

Type the number of a device to disable and a return, then type: **1 [cr]** to disable the testing.
Next type **0 [cr]**, to return to the ‘Device Menu’.

When you have completed device disabling, type: **0 [cr]** this will return you to the ‘Service Menu’.

At the ‘Service Menu’ type: **2 [cr]** to start the system exerciser. The program will pause and wait for confirmation for any device that requires that a loop-back be installed. Type **[cr]** to confirm the request or type a **Ctrl C** to stop the process and return to the ‘Service Menu’. After loop-back confirmation completes, each device will perform a function test and then all devices will have their exercisers started and they will run concurrently until an error is encountered or testing is terminated by typing a **Ctrl C**.

# 9. Verify installation in a PDPq system

This step describes how to verify installation of the DQP-1400 in a PDPq system. The DQP-1400 is supplied with a CAB-1402-12 loop-back cable to allow you to run Digital's XXDP diagnostics as described below. Install CAB-1402-12 must be installed between J1 and J2 when running the diagnostics. **Note that the cable is built to install with a 180 degree twist.**

The DQP-1400 diagnostic software is designated as follows:

- VDRCC0 Part 1
- VDRDB0 Part 2
-

The following conventions are used below:

`output` In examples, computer output is shown in this type.

**`user input`** In examples, user input is shown in bold type.

A. NuPDP is shipped and configured to use a DEC standard, VT100-style terminal and requires CAB-2009-18 or CAB-2010-18 as an adapter cable between the NuPDP serial port and the DEC terminal cable. Terminal emulators or simple character terminals can plug directly into the NuPDP DE9 COM port using a standard cross-over cable and do not require an adapter cable.

B. Open the drive access door and ensure that the system drive cartridge is locked. Keys to the cartridge are supplied with the system.

C. Power up the system. The console displays:

```
Type y to boot XXDP else the OS boots in 4 seconds [Y,N]?Y

BOOTING UP XXDP-XM EXTENDED MONITOR

XXDP-XM EXTENDED MONITOR – XXDP V2.5
REVISION: F0
BOOTED FROM DL0
124KW OF MEMORY
NON-UNIBUS SYSTEM

RESTART ADDRESS: 152000
TYPE “H” FOR HELP !
.
```

D. To run the diagnostic type:

**R VDRCC0 <cr>**

The diagnostic begins and displays the following:

CVDRCC DRV11J DIAG TEST PART 1

DRV11 CABLE REQ'D

SWR = 000000 NEW =

E. Enter: **100000<cr>**
If no errors occur the program will start displaying END PASS # messages.

F. Allow a minimum of 10 error free passes.

G. Type CTRL P to display the NuPDP prompt, type HALT to stop the diagnostic. To restart XXDP, type Boot DL0

H. To run part 2 of the DQP-1400 diagnostic, type:

**R VDRDB0 <cr>**
The diagnostic begins and displays the following:

CVDRDB DRV11J DIAG TEST PART 2

DRV11J CABLE REQ'D

SWR = 000000 NEW =

I. Enter: **100000<cr>**
The diagnostic continues running unless an error halt occurs. As the test runs, the program displays END PASS # messages.

J. Allow a minimum of 20 error free passes.

If any error is reported, check to ensure that the loop-back cable is installed correctly. If the loop-back cable and DQP-1300 are both installed correctly and an error is reported, please contact customer support with error information.

K. To exit the diagnostic:
1. Restart the system by pressing the Reset button or cycling power, or
2. Type CTRL P to display the NuPDP prompt, type HALT to stop the diagnostic. To restart XXDP, type Boot DL0

# 2 General Description

## Product Description

The DQP-1400 is a dual-width parallel line interface module designed for use in NuVAX and NuPDPq systems. It takes advantage of today's FPGA technology to emulate the functionality of DEC's DRV11-J parallel line interface module. The DQP-1400 contains four programmable ports designated A, B, C and D. Each port contains sixteen I/O lines and is capable of transferring a 16-bit word between the PCI bus and the user device(s). Data word transfers in or out of the DQP-1400 are accomplished by the assertion of two control signals at each port of the DQP-1400 and two control signals asserted by the user device to its respective port. These control signals must be asserted in a protocol sequence while observing timing constraints to ensure an orderly data transfer.

The DQP-1400 will also accept interrupt requests from up to sixteen I/O lines. This interrupt capability makes it useful for sensor I/O applications.

The DQP-1400 may also be used as a general purpose parallel interface to custom devices or DQP-1400s may be connected together as a link between PCI buses.

The DQP-1400 contains two programmable mode registers that provide a number of operating modes to customize the module configuration for different system applications. The module may be programmed for use in vectored-interrupt-driven systems or software-polled systems. When used in vectored interrupt systems, the module may be programmed to operate in either a fixed or rotating priority mode with a single common or individual vectors in response to user device(s) interrupt requests. Additional operating options available under program control include the selection of an active high or active low interrupt request polarity, pre-selection of internal registers, and the selection of a master mask bit to arm or disarm the interrupt capability of the DQP-1400.

The DQP-1400 also contains two RAMS that are used to store programmed interrupt vectors. One 8-bit RAM location is used to store an interrupt vector. One vector may be programmed for each of the 16 interrupt request inputs.

# Features

- Four 3-state, 16-bit parallel I/O ports
- Acceptance of up to 16 external interrupt requests
- Program-controlled input/output operations
- Programmable operating modes:
  Interrupt Controller Mode - Interrupt-driven or polled
  Priority Modes - Fixed or Rotating

# Specifications

### Physical Dimensions

| | |
|---|---|
| DQP-1400-A Controller | Standard short card measuring 6.875 inches by 4.2 inches (17.46 cm by 10.67 cm) |
| CPX-1403 Panel | 7.75 inches by 4.00 inches by .68 inches (19.69 cm by 10.16 cm by 1.72 cm) |

### Interface

| | |
|---|---|
| Controller to Cable: | 100-pin high density connector |
| Adapter Cable: | 8-foot, terminated with a 100-pin connector at each end. |

### Electrical

Power Required:

| | |
|---|---|
| +5volts | 0.5 amps |
| +3.3 volts | 0.4 amps |

Bus Loading 2 ac loads, 1 dc load

I/O Signal Parameters:

Data Buffer 3-State Outputs

V(OL) = 0.5V @ I(OL) = 8mA
V(OL) = 0.4V @ I(OL) = 4mA
V(OH) = 2.4V @ I(OH) = -2.6mA

Data Buffer Inputs

I(IL) = -0.2mA @ V(IL) = 0.4V
V(IH) = 20µA @ V(IH) = 2.7V

Protocol Signal 3-State Outputs

V(OL) - 0.55V @ I(OL) = 64mA
V(OH) - 2.4 @ I(OH) = -15mA

Protocol Signal Inputs

Termination = 120Ω
I(IL) = -27mA @ V(IL) = 0.5V
I(IH) = 80µA @ V(IH) = 2.7V

## Environmental

Operating Conditions:

| | |
|---|---|
| Temperature | 5° to 50° C (41° to 122° F) |
| Relative Humidity | 20% to 80% non-condensing |

Storage Conditions:

| | |
|---|---|
| Temperature | -40° to 66° C (-40° to 150° F) |
| Relative Humidity | 10% to 95% non-condensing |

# 3 Registers

## General Description

The DCQ-1400 contains the logic necessary to provide communication between the DQP-1400 and up to four user devices in 16-bit word lengths via four I/O ports. Four control lines associated with each of the four ports ensure orderly information transfers. Word transfers are executed by programmed I/O operations or interrupt-driven routines. Write data is output by the DCQ-1400 to the I/O bus through 3-state data latches, and read data is input through unlatched bus buffers.

All control/status and I/O data transfers take place over a bi-directional internal bus (DB bits 15- 00) on the DCQ-1400. The module contains four I/O buses, one for each port (A, B, C and D). Each port has an associated control/status register (CSRA, CSRB, CSRC or CSRD) that contains status information when read and command words when written. All ports have 16 bi-directional 3-state lines and perform controlled input/output operations. Note that port A is the only port that will perform bit interrupt functions in addition to input/output data transfers. The 16 external interrupt requests are functionally divided into two groups of eight lines, referred to as group 1 and group 2.

## Control/Status Registers

The control/status registers (CSRA, CSRB, CSRC and CSRD) are read/write byte-addressable registers with bit assignments as shown in Figures 3-1 through 3-4. The function and description of the control/status register bits are described in Tables 3-1 through 3-4.

## Control/Status Register A (CSRA)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY A | | | | | | IE | DIR A | C/S 7 | C/S 6 | C/S 5 | C/S 4 | C/S 3 | C/S 2 | C/S 1 | C/S 0 |

Figure 3-1: Control/Status Register A Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | C/S 7 - C/S 0 | Read/Write | CSR A bits 07-00. These bits are used in conjunction with CSR B bits 07-00 to program interrupt control group 1. They contain status information when read and command words when written. Unaffected by BINIT. |
| 08 | DIR A | Read/Write | Direction A. Used for controlling DBRA. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCQ-1400 RDY output signal is asserted and the DCQ-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCQ-1400 is the output device. The negation of either DIR or USER RDY causes the DCQ-1400 outputs to remain in their high impedance state. Cleared by BINIT. |
| 09 | IE | Read/Write | Interrupt Enable. Enables the DCQ-1400 to generate processor interrupts when set. Used to enable both group 1 and group 2 interrupts. Cleared by BINIT. |
| 14-10 | NU | | Not used. Read as all zeroes. |
| 15 | RDY A | Read only | User Ready A. Used to control DBRA. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCQ-1400 output operations. The user device asserts this signal when it desires the DCQ-1400 to output data. Unaffected by BINIT. |

Table 3-1: CSRA Bit Functions and Descriptions

## Control/Status Register B (CSRB)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY B | | | | | | | DIR B | D 7 | D 6 | D 5 | D 4 | D 3 | D2 | D 1 | D0 |

Figure 3-2: Control/Status Register B Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | D 7 - D 0 | Read/Write | CSR B bits 07-00. These bits are used in conjunction with CSR A bits 07-00 to program interrupt control group 1. They contain information selected by the command word loaded through CSRA. The registers available are the IRR, ISR, ACR, IMR and the vector address memory. Unaffected by BINIT. |
| 08 | DIR B | Read/Write | Direction B. Used for controlling DBRB. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCQ-1400 RDY output signal is asserted and the DCQ-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCQ-1400 is the output device. The negation of either DIR or USER RDY causes the DCQ-1400 outputs to remain in their high impedance state. Cleared by BINIT. |
| 14-09 | NU | | Not used. Read as all zeroes. |
| 15 | RDY B | Read only | User Ready B. Used to control DBRB. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCQ-1400 output operations. The user device asserts this signal when it desires the DCQ-1400 to output data. Unaffected by BINIT. |

Table 3-2: CSRB Bit Functions and Descriptions

## Control/Status Register C (CSRC)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY C | | | | | | | DIR C | C/S 7 | C/S 6 | C/S 5 | C/S 4 | C/S 3 | C/S 2 | C/S 1 | C/S 0 |

Figure 3-3: Control/Status Register C Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | C/S 7 - C/S 0 | Read/Write | CSR C bits 07-00. These bits are used in conjunction with CSR D bits 07-00 to program interrupt control group 1. They contain status information when read and command words when written. Unaffected by BINIT. |
| 08 | DIR C | Read/Write | Direction C. Used for controlling DBRC. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCQ-1400 RDY output signal is asserted and the DCQ-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCQ-1400 is the output device. The negation of either DIR or USER RDY causes the DCQ-1400 outputs to remain in their high impedance state. Cleared by BINIT. |
| 14-09 | NU | | Not used. Read as all zeroes. |
| 15 | RDY C | Read only | User Ready C. Used to control DBRC. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCQ-1400 output operations. The user device asserts this signals when it desires the DCQ-1400 to output data. Unaffected by BINIT. |

Table 3-3: CSRC Bit Functions and Descriptions

## Control/Status Register D (CSRD)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY D | | | | | | | DIR D | D 7 | D 6 | D 5 | D 4 | D 3 | D2 | D 1 | D0 |

Figure 3-4: Control/Status Register D Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | D 7 - D 0 | Read/Write | CSR D bits 07-00. These bits are used in conjunction with CSR C bits 07-00 to program interrupt control group 2. They contain information selected by the command word loaded through CSRC. The registers available are the IRR, ISR, ACR, IMR and the vector address memory. Unaffected by BINIT. |
| 08 | DIR D | Read/Write | Direction D. Used for controlling DBRD. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCQ-1400 RDY output signal is asserted and the DCQ-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCQ-1400 is the output device. The negation of either DIR or USER RDY causes the DCQ-1400 outputs to remain in their high impedance state. Cleared by BINIT. |
| 14-09 | NU | | Not used. Read as all zeroes. |
| 15 | RDY D | Read only | User Ready D. Used to control DBRD. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCQ-1400 output operations. The user device asserts this signal when it desires the DCQ-1400 to output data. Unaffected by BINIT. |

Table 3-4: CSRD Bit Functions and Descriptions

# Data Buffer Registers

The four data buffer registers (DBRA, DBRB, DBRC and DBRD) are 16-bit word-addressable registers. They are used as latched output data buffers when the DCQ-1400 is in output mode (write) and as unlatched bus buffers in input mode (read). The contents of the output data buffers may be examined while the DCQ-1400 is in an output mode by performing a read operation of the input data buffers. This ability to examine the output data buffers in the output mode provides software access to the internal conditions of the DCQ-1400.

The latched output data buffer registers DBRA through DBRD are not cleared by BINIT. The bit assignment is the same for all registers and is shown in Figure 3-5.

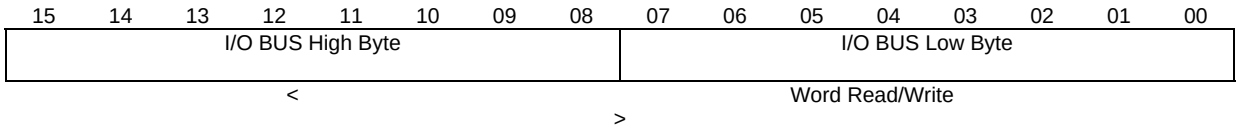



Figure 3-5: Data Buffer Register Bit Assignments

# Interrupt Control

The DCQ-1400 is capable of monitoring 16 lines to generate 16 vectored interrupts. Functional and operating descriptions of the signals required to initiate interrupts and the DCQ-1400 registers used for programming are provided in the sections below.

### Functional Description

Five Qbus control signals are used by the interrupt control logic for initialization, sending interrupt requests to the processor, receiving the interrupt acknowledge signal from the processor and sending the vector address to the processor: BIRQ4, BIAKI, BRPLY, BDIN and BINIT.

There are two interrupt controllers on the DCQ-1400. Each controller is responsible for monitoring a group of eight interrupt request inputs. Each group of eight interrupt requests is applied via IRQ buffers to an 8-bit interrupt request register (IRR) in the interrupt controller.

The two interrupt controllers (group 1 and group 2) are programmed independently. The group 1 interrupt controller is programmed through the low bytes of CSRA and CSRB while the group 2 interrupt controller is programmed through the low bytes of CSRC and CSRD. The only commonalities of the two groups are priority resolution and the interrupt enable (IE) CSRA bit 9. Both interrupt controllers must operate in the same mode, either interrupt or polled. Each interrupt controller contains an 8-bit interrupt mask register (IMR) that may be used to disable the processing of any undesired interrupt requests.

The group 1 interrupt controller has the higher priority and its enable output is connected to the enable input of group 2. Group 1 must be armed to accept interrupts with the master mask bit set in the mode register. When group 1 is armed, its enable output goes high, thus enabling group 2 interrupts. Therefore, whenever the interrupt mode is selected, group 1 must be armed, even if none of the group 1 interrupt requests are being used in order to pass the enable signal along to group 2.

Group 1 and group 2 may be programmed to respond to either an active high or an active low transition on the interrupt request lines. A bit in the interrupt request register (IRR) is set whenever the corresponding interrupt request line makes an inactive-to-active transition and meets the active pulse width requirements. Active pulse widths 270ns or greater set the corresponding IRR bit, while pulse widths of 30ns or less are ignored. Active pulse widths between 30ns and 270ns may or may not set the IRR bit.

### Interrupt Controller Interface

Each interrupt controller group accepts eight IRQ inputs through the IRQ buffers. When an active interrupt, for example IRQ7, is applied to group 1, a group interrupt (GINT) is generated if the request is not masked or the master mask bit has not disarmed the interrupt controller. The GINT signal generates BIRQ4 if the processor has enabled interrupts by setting the interrupt enable bit. The processor accepts BIRQ4 after executing the current instruction, issues BIAK, and disables its internal interrupt structure. When the processor returns the BIAK signal, the DCQ-1400 blocks it from being transmitted to devices further down the bus. The interrupt controllers perform priority arbiration to select the highest unmasked pending interrupt and then outputs a vector address associated with the selected interrupt request. When the interrupt acknowledge sequence begins, the highest priority unmasked request is latched so that any higher requests that may be received during the present interrupt sequence doesn't cause confusion and cause the wrong vector to be transmitted.

### Interrupt Controller Operating Description

Interrupt requests IRQ7-IRQ0 are captured and latched in the interrupt request register (IRR). Any requests not masked by the interrupt mask register (IMR) cause a group interrupt (GINT) output to the processor if the interrupt controller is enabled, armed and IE (CSRA) bit 9 is set. When the processor is ready to accept the interrupt, it issues an IAKL pulse that initiates two operations. First, the priority of pending interrupts is resolved, and second, the vector address associated with the highest priority interrupt is transferred from the vector address memory to the data bus.

Other interrupt management functions are controlled by the auto-clear register (ACR), the interrupt service register (ISR), and the mode register (MR). The command register is used by the processor to exercise control over the many functions provided by the DCQ-1400 while the status register reports on the internal condition of the DCQ-1400.

Each interrupt controller is addressed by the processor as either a control port or a data port. The control port provides direct access to the command register and the status register. The data port is used to communicate with all other internal locations.

Information is transferred through the interrupt controller, the DCQ-1400 I/O bus, and the Qbus by the eight 3-state bi-directional data bus lines

The status register is selected directly for reading by the control input. Other internal registers are read by pre-selecting the desired register with mode bits 5 and 6, and then executing a data read. The vector address memory can be read only with IAK pulses.

The command register is selected directly for writing by the control input. The mask and auto-clear registers are loaded following specific commands to that effect. To load each level (IRQ7-IRQ0) of the vector address memory, the vector address memory pre-select command is issued to select the desired level. A data-write operation is then executed to load that level.

## Interrupt Control Reset

The DCQ-1400 does not include an external hardware reset input for the interrupt control. The reset function is accomplished by software command, or automatically during power-up. The processor may initiate a reset at any time by writing all 0s into the command register of each interrupt controller. Power-up reset circuitry on each interrupt controller integrated circuit is internally triggered by the rising $V_{CC}$ voltage (IC supply voltage 5V) to generate a brief reset pulse when the predetermined threshold is reached. The interrupt controllers are unaffected by a BINIT on the Qbus.

The vector address memory contents are cleared by BINIT. Therefore, if the vector address memory is to be used, it must be initialized by the processor after power-up.

The interrupt mask register is set to all 1s by either a software reset or a power-up reset, thus disabling recognition of interrupts by the DCQ-1400. The status registers continue to reflect the internal condition of group 1 and group 2 and are not otherwise affected by a reset.

The mode registers are cleared to all 0s to provide the DCQ-1400 with a reasonable operating environment after a power-up or software reset. The mode registers after reset are assigned to following options:

Interrupt mode
Individual vectoring
Fixed interrupt priority
IRQ polarity active low
ISR pre-selected for reading
Interrupt controllers disarmed by master mask bit

## Interrupt Control Register Description

The DCQ-1400 uses the control and operation registers, plus the vector address memories of the interrupt controllers to perform and manage its many functions. Table 3-5 lists these elements and summarizes their size and number.

| Description | Register Abbreviation | Bits Size per Register | Quantity per DCQ-1400 |
|---|---|---|---|
| Interrupt request register | IRR | 8 | 2 |
| Interrupt service register | ISR | 8 | 2 |
| Interrupt mask register | IMR | 8 | 2 |
| Auto-clear register | ACR | 8 | 2 |
| Status register | - | 8 | 2 |
| Mode register | - | 8 | 2 |
| Command register | - | 8 | 2 |
| Vector address memory | - | 8x8* | 16 |

*Each interrupt controller contains 8 vector address memory locations of 8 bits each.

Table 3-5: Interrupt Control Register and Memory Summary

## Status Register

Each status register is eight bits wide and contains information describing the internal state of the DCQ-1400. The status register is read directly by executing a read operation at CSRA for group 1 or CSRC for group 2. Figure 3-6 shows the status register bit assignments.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| S7 | S6 | S5 | S4 | S3 | S2-S0 | | |

Figure 3-6: Status Register Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07 | S7 | | Group Interrupt.<br>1 = No unmasked IRR bit set<br>0 = At least one unmasked IRR bit set<br>This bit reflects the information state of the group interrupt (GINT) signal. Bit S7 remains valid when interrupts are disabled by the polled mode option, thus permitting the processor to check for interrupts by reading the status register. |
| 06 | S6 | | Enable Input (Group 2 only)<br>0 = Disabled<br>1= Enabled<br>This bit reflects the state of the enable-in (EI) input signal and indicates if group 2 is enabled or disabled. When S6 is high, group 2 can generate an interrupt request. When S6 is low, group 2 interrupt requests are disabled. Group 1 is always enabled. |
| 05 | S5 | | Priority Mode<br>0 = Fixed<br>1 = Rotating<br>This bit reflects the state of the priority mode option as specified by mode register bit M0. When S5 is high, rotating priority is selected. When S5 is low, fixed priority is selected. |

Table 3-6: Status Register Bit Functions

| Bit | Name | Function | Description |
|---|---|---|---|
| 04 | S4 | | Interrupt Mode<br>0 = Interrupt<br>1 = Polled<br>This bit reflects the state of the interrupt mode option as specified by mode register bit 2. When S4 is high, the polled mode is selected and interrupt requests are disabled. When S4 is low, the interrupt mode is selected. |
| 03 | S3 | | Master Mask Bit<br>0 = Disarmed<br>1 = Armed<br>This bit reflects the state of the master mask bit as specified by mode register bit M7. When S3 is low, the group is disarmed and IRR bits that are set do not generate interrupt requests. When S3 is high, the group is armed and interrupts can occur. |
| 02-00 | S2-S0 | | For internal use only. May read as zeros or ones. |

Table 3-6: Status Register Bit Functions (cont'd)

## Command Register

Each command register is eight bits wide and is used to store the most recently entered command. The register is loaded directly from the data bus by executing a write operation at CSRA for group 1 or CSRC for group 2. Depending on the specific command opcode that is entered, an immediate internal activity may be initiated, or CSRB and CSRD may be pre-conditioned for subsequent register transfers. The opcodes for each command operation are described in the "Command Descriptions" section later in this chapter.

## Mode Register

Each mode register is eight bits wide and is used to establish the operating modes and conditions for the many functional features of the DCQ-1400. The mode register allows the processor to customize the interrupt system for a particular application. Figure 3-7 shows the mode register bit assignments. No single command or interface operation loads all bits of the mode command register. Mode bits M5, M6 and M7 are controlled by separate commands. The mode register contents cannot be read out on the data bus. However, the conditions of mode bits M0, M2 and M7, which reflect the priority, interrupt and master mask bit modes, are available as part of the status register. The mode register is cleared by a software reset or a power-up reset.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |

Figure 3-7: Mode Register Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07 | M7 | Master Mask Bit | 0 = Disarmed<br>1 = Armed |
| 06-05 | M6-M5 | | Register Pre-selection<br>00 = Interrupt service<br>01 = Interrupt mask<br>10 = Interrupt request register<br>11 = Auto clear register |
| 04 | M4 | | Ireq Polarity<br>0 = Active low<br>1 = Active High |
| 03 | M3 | | Unused. Must be 0. |
| 02 | M2 | | Interrupt mode<br>0 = Interrupt<br>1 = Polled |
| 01 | M1 | | Vector Selection<br>0 = Individual vector<br>1 = Common vector |
| 00 | M0 | | Priority Mode.<br>0 = Fixed<br>1 = Rotating |

Table 3-7: Mode Register Bit Functions

## Interrupt Request Register (IRR)

Each IRR is eight bits wide and is used to recognize and store active transitions on the eight interrupt request lines. A bit in the IRR is set whenever the corresponding IRQ input line makes an inactive-to-active transition and meets the minimum active pulse width requirements. Also, the processor (under program control) may set the IRR bits by using two types of commands. This capability permits software-initiated interrupts and is a useful tool for system testing.

All IRR bits are cleared by a reset. Individual IRR bits are cleared automatically when their interrupts are acknowledged by the processor. Four types of commands, in addition to reset, allow the processor to clear IRR bits.

The IRR may be read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CSRB bits 7-0 for group 1 or CSRD bits 7-0 for group 2.

**Interrupt Service Register (ISR)**

Each ISR is eight bits wide and is used to store the acknowledge status of individual interrupts. When the processor acknowledges an interrupt request, the DCQ-1400 selects the highest priority request that is pending, clears the asociated IRR bit, and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing, it is reset by the internal hardware before the end of the acknowledge sequence. When the ISR bit is not programmed for automatic clearing, it must be reset by command from the processor.

The DCQ-1400 uses the ISR internally to erect a "masking fence." When an ISR bit is set and fixed priority mode is selected, only requests of higher priority causes a new group interrupt (GINT) output. Thus, requests from lower priority interrupts (and from new requests associated with the set ISR bit) will be "fenced out" and ignored until the ISR bit is cleared. In the rotating priority mode, all requests are fenced out by an ISR bit that is set and no new interrupts are generated until the ISR bit is cleared. When automatic clearing is specified, no masking fence is erected since the ISR bit is cleared.

When in the fixed mode, if an unmasked interrupt arrives from a device of higher priority than the current ISR, the processor will be interrupted if its interrupt input is enabled. When the new interrupt is acknowledged, the associated higher priority ISR bit is set and the fence moves up to the new priority level. When the new ISR bit is cleared, the fence will then fall back to the previous ISR level. The ISR may be read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CSRB (bits 7-0) for group 1 or CSRD (bits 7-0) for group 2.

**Interrupt Mask Register (IMR)**

Each IMR is eight bits wide and is used to enable/disable the processing of individual interrupts. Only unmasked IRR bits can generate an interrupt. The IMR does not otherwise affect the operation of the IRR. An IRR bit that is set while masked will cause an interrupt when its IMR bit is cleared.

All eight IMR bits for each group may be set, cleared, read or loaded in parallel by the processor. In addition, individual IMR bits may be set or cleared by command. This allows a control routine to enable or disable directly an individual interrupt without disturbing the other mask bits and without knowledge of their state or context.

The IMR polarity is active high for masking: a 0 enables the interrupt and a 1 disables it. The power-on reset and the software reset cause all IMR bits to be set, thus disabling all interrupt requests. The IMR may be read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CSRB (bits 7-0) for group 1 or CSRD (bits 7-0) for group 2.

## Auto-Clear Register (ACR)

Each ACR is eight bits wide and specifies the automatic clearing option for each of the ISR bits. When an auto-clear bit is set, the corresponding ISR bit set in an interrupt acknowledge (IAK) cycle is cleared by the internal hardware before the end of the IAK sequence. When an auto-clear bit is not set, the corresponding ISR bit that has been set in an IAK cycle is cleared by a command from the processor.

When selected, the auto-clear option provides two related functional effects. First, it eliminates the need for the associated interrupt service routine to issue a command to clear the ISR bit. Second, it eliminates the masking fence that would otherwise have been erected, allowing lower priority interrupts to cause a new interrupt request.

The ACR is loaded in parallel from the data bus by issuing the ACR load pre-select command, followed by a write into the data port. The ACR is read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CRSB (bits 7-0) for group 1 or CSRD (bits 7-0) for group 2.

## Vector Address Memory

The vector addresses are programmed by the vector address memory pre-select command, followed by a data-write operation to load the vector address required for each interrupt request level. The vector address memory pre-select command is entered directly into the low byte (bits 7-0) of CSRA for group 1 or the low byte (bits 7-0) of CSRC for group 2. Pre-select commands entered through CSRA select CSRB for subsequent loading of the vector addresses in group 1. Pre-select commands entered through CSRC select CSRD to load the addresses for group 2.

Normally, one vector address is loaded after each pre-selection command. Figure 1-3 shows the vector bit positions relative to the loaded byte. This in turn causes one interrupt to occur for each valid transition on the corresponding IRQ input. Vector addresses are placed on the Qbus during IAK operation.

Loading the vector address into each new interrupt request level must be preceded by a new vector address memory pre-select command. Therefore, 16 pre-select commands, each followed by a data-write operation, are required to load 16 vector addresses into the vector address memory.

The DCQ-1400 only uses one vector address per interrupt. To ensure proper operation, load only one data byte after each pre-select command.

# Appendix A
# PCI Local Bus Interface Connector Pin Assignments

This appendix lists the pin assignments for the PCI bus interface.

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| A1 | TRST-L | B1 | -12V |
| A2 | +12V | B2 | TCK-H |
| A3 | TMS-H | B3 | GND |
| A4 | TDI-H | B4 | TDO-H |
| A5 | +5V | B5 | +5V |
| A6 | INTA-L | B6 | +5V |
| A7 | INTC-L | B7 | INTB-L |
| A8 | +5V | B8 | INTD-L |
| A9 | | B9 | PRSNT1-L |
| A10 | +5V | B10 | |
| A11 | | B11 | PRSNT2-L |
| A12 | GND | B12 | GND |
| A13 | GND | B13 | GND |
| A14 | | B14 | |
| A15 | RST-L | B15 | GND |
| A16 | +5V | B16 | CLK-H |
| A17 | GNT-L | B17 | GND |
| A18 | GND | B18 | REQ-L |
| A19 | | B19 | +5V |
| A20 | AD30-H | B20 | AD31-H |
| A21 | +3.3V | B21 | AD29-H |
| A22 | AD28-H | B22 | GND |
| A23 | AD26-H | B23 | AD27-H |
| A24 | GND | B24 | AD25-H |
| A25 | AD24-H | B25 | +3.3V |
| A26 | IDSEL-H | B26 | C/BE3-L |
| A27 | +3.3V | B27 | AD23-H |
| A28 | AD22-H | B28 | GND |
| A29 | AD20-H | B29 | AD21-H |
| A30 | GND | B30 | AD19-H |

Table A-1: PCI Bus Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| A31 | AD18-H | B31 | +3.3V |
| A32 | AD16-H | B32 | AD17-H |
| A33 | +3.3V | B33 | C/BE2-L |
| A34 | FRAME-L | B34 | GND |
| A35 | GND | B35 | IRDY-L |
| A36 | TRDY-L | B36 | +3.3V |
| A37 | GND | B37 | DEVSEL-L |
| A38 | STOP-L | B38 | GND |
| A39 | +3.3V | B39 | LOCK-L |
| A40 | SDONE-H | B40 | PERR-L |
| A41 | SBO-L | B41 | +3.3V |
| A42 | GND | B42 | SERR-L |
| A43 | PAR-H | B43 | +3.3V |
| A44 | AD15-H | B44 | C/BE1-L |
| A45 | +3.3V | B45 | AD14-H |
| A46 | AD13-H | B46 | GND |
| A47 | AD11-H | B47 | AD12-H |
| A48 | GND | B48 | AD10-H |
| A49 | AD09-H | B49 | GND |
| A50 | KEYWAY | B50 | KEYWAY |
| A51 | KEYWAY | B51 | KEYWAY |
| A52 | C/BE0-L | B52 | AD08-H |
| A53 | +3.3V | B53 | AD07-H |
| A54 | AD06-H | B54 | +3.3V |
| A55 | AD04-H | B55 | AD05-H |
| A56 | GND | B56 | AD03-H |
| A57 | AD02-H | B57 | GND |
| A58 | AD00-H | B58 | AD01-H |
| A59 | +5V | B59 | +5V |
| A60 | REQ64-L | B60 | ACK64-L |
| A61 | +5V | B61 | +5V |
| A62 | +5V | B62 | +5V |

Table A-1: PCI Bus Pin Assignments (cont'd)

# Appendix B
# User Connector Pin Assignments

Two board 50-pin male connectors (J1 and J2) interface the CPX-1403 panel to the user device. Connector J1 is used to interface the port A and port B signals, while J2 is used for the port C and port D signals. Figure A-1 shows the connector, Table B-1 lists the interface signal names and their pin numbers.

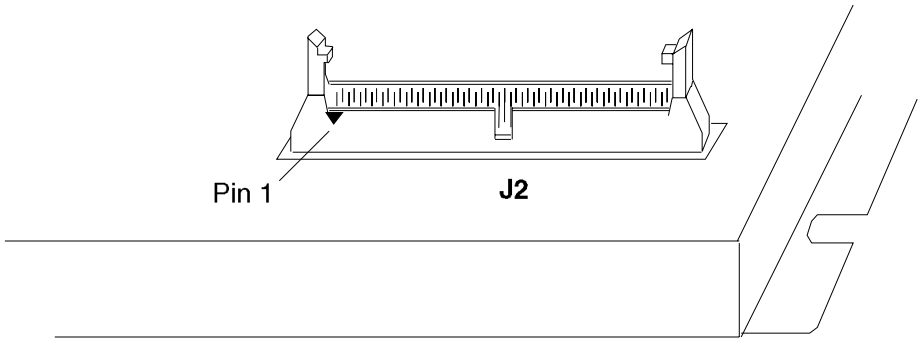



Figure B-1: CPX-1403 User Connector

| Signal Name | J1 Connector Pin | J1 Connector Pin | Signal Name |
|---|---|---|---|
| B_09 | 1 | 2 | B_12 |
| B_11 | 3 | 4 | B_08 |
| B_14 | 5 | 6 | B_15 |
| B_10 | 7 | 8 | B_13 |
| B_05 | 9 | 10 | B_07 |
| B_03 | 11 | 12 | B_01 |
| B_02 | 13 | 14 | B_00 |
| B_06 | 15 | 16 | B_04 |
| GND | 17 | 18 | B_URPLY |
| GND | 19 | 20 | B_DVRDY |
| GND | 21 | 22 | B_URDY |
| GND | 23 | 24 | B_DVRPLY |
| GND | 25 | 26 | GND |
| A_URPLY | 27 | 28 | GND |
| A_DVRDY | 29 | 30 | GND |
| A_URDY | 31 | 32 | GND |
| A_DVRPLY | 33 | 34 | GND |
| A_04 | 35 | 36 | A_06 |
| A_00 | 37 | 38 | A_02 |
| A_01 | 39 | 40 | A_03 |
| A_07 | 41 | 42 | A_05 |
| A_13 | 43 | 44 | A_10 |
| A_15 | 45 | 46 | A_14 |
| A_08 | 47 | 48 | A_11 |
| A_12 | 49 | 50 | A_09 |

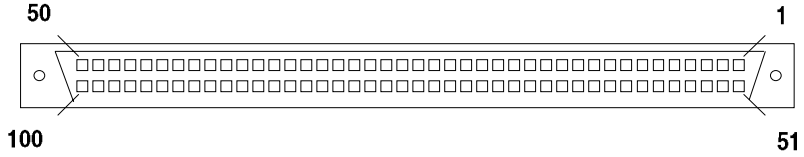
Table B-1: User Connector Pin Assignments

| Signal Name | J2 Connector Pin | J2 Connector Pin | Signal Name |
|---|---|---|---|
| C_09 | 1 | 2 | C_12 |
| C_11 | 3 | 4 | C_08 |
| C_14 | 5 | 6 | C_15 |
| C_10 | 7 | 8 | C_13 |
| C_05 | 9 | 10 | C_07 |
| C_03 | 11 | 12 | C_01 |
| C_02 | 13 | 14 | C_00 |
| C_06 | 15 | 16 | C_04 |
| GND | 17 | 18 | C_URPLY |
| GND | 19 | 20 | C_DVRDY |
| GND | 21 | 22 | C_URDY |
| GND | 23 | 24 | C_DVRPLY |
| GND | 25 | 26 | GND |
| D_URPLY | 27 | 28 | GND |
| D_DVRDY | 29 | 30 | GND |
| D_URDY | 31 | 32 | GND |
| D_DVRPLY | 33 | 34 | GND |
| D_04 | 35 | 36 | D_06 |
| D_00 | 37 | 38 | D_02 |
| D_01 | 39 | 40 | D_03 |
| D_07 | 41 | 42 | D_05 |
| D_13 | 43 | 44 | D_10 |
| D_15 | 45 | 46 | D_14 |
| D_08 | 47 | 48 | D_11 |
| D_12 | 49 | 50 | D_09 |

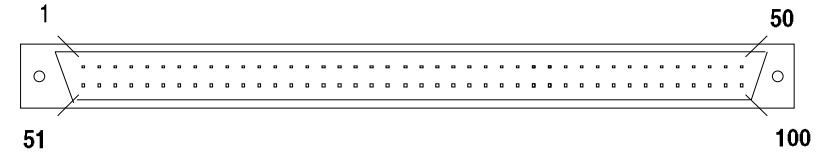
Table B-1: User Connector Pin Assignments (Cont'd)

# Appendix C
# Interconnect Cable Pin Assignments

This appendix lists the pin assignments for the interconnect cable between the DQP-1400 controller and the CPX-1403-A panel. The connectors at both ends of the interconnect cable are 100-pin high density SCSI style cable plugs. The connectors on the modules are SCSI style receptacles, AMP part number 749076-9 or Thomas & Betts Ansley part number HFR100RA29BX1. The pin assignments are listed below.




**100-pin High Density Receptacle**




**100-pin High Density Cable Plug**

**DQP-1400 Connector J1**
**CPX-1403 Connector J3**

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| GND | 1 | 51 | GND |
| A_URPLY | 2 | 52 | A_DVRPLY |
| GND | 3 | 53 | GND |
| A_URDY | 4 | 54 | A_DVRDY |
| A_08 | 5 | 55 | A_00 |
| A_09 | 6 | 56 | A_01 |
| A_10 | 7 | 57 | A_02 |
| A_11 | 8 | 58 | A_03 |
| A_12 | 9 | 59 | A_04 |
| A_13 | 10 | 60 | A_05 |
| A_14 | 11 | 61 | A_06 |
| A_15 | 12 | 62 | A_07 |
| GND | 13 | 63 | GND |
| B_URPLY | 14 | 64 | B_DVRPLY |
| GND | 15 | 65 | GND |
| B_URDY | 16 | 66 | B_DVRDY |
| B_08 | 17 | 67 | B_00 |
| B_09 | 18 | 68 | B_01 |
| B_10 | 19 | 69 | B_02 |
| B_11 | 20 | 70 | B_03 |
| B_12 | 21 | 71 | B_04 |
| B_13 | 22 | 72 | B_05 |
| B_14 | 23 | 73 | B_06 |
| B_15 | 24 | 74 | B_07 |
| GND | 25 | 75 | GND |
| C_URPLY | 26 | 76 | C_DVRPLY |
| GND | 27 | 77 | GND |
| C_URDY | 28 | 78 | C_DVRDY |
| C_08 | 29 | 79 | C_00 |
| C_09 | 30 | 80 | C_01 |
| C_10 | 31 | 81 | C_02 |
| C_11 | 32 | 82 | C_03 |
| C_12 | 33 | 83 | C_04 |
| C_13 | 34 | 84 | C_05 |
| C_14 | 35 | 85 | C_06 |
| C_15 | 36 | 86 | C_07 |
| GND | 37 | 87 | GND |
| D_URPLY | 38 | 88 | D_DVRPLY |
| GND | 39 | 89 | GND |
| D_URDY | 40 | 90 | D_DVRDY |
| D_08 | 41 | 91 | D_00 |
| D_09 | 42 | 92 | D_01 |
| D_10 | 43 | 93 | D_02 |
| D_11 | 44 | 94 | D_03 |
| D_12 | 45 | 95 | D_04 |
| D_13 | 46 | 96 | D_05 |
| D_14 | 47 | 97 | D_06 |
| D_15 | 48 | 98 | D_07 |
| GND | 49 | 99 | GND |
| GND | 50 | 100 | GND |

Table C-1: DQP-1400 to CPX-1403 Interconnect Cable Pin Assignments

75 Gateway Blvd.
Cottage Grove, Oregon 97424 USA
http://www.logical-co.com

The Logical Company

Telephone: +1 541-942-3610
Fax: +1 541-942-3640
E-mail: sales@logical-co.com