# DCE-1400
# DRV11-J Compatible Interface for the PCI Express Bus
## Owner's Manual

**DCE-1400-OM**
**Revision B**

# Owner's Manual for the

# DCE-1400

**DRV11-J Compatible Interface for the PCI Express Bus**

The **Logical** Company

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# 1 Installation

This chapter lists the steps involved in installing the DCE-1400 hardware. References throughout this chapter tell you where to look for more detailed information. The DCE-1400 module is shown in Figure 1-1 and the CPX-1403 adapter panel in Figure 1-2. Refer to these figures as you follow the steps outlined below.

The switch pack at U21 and the six jumpers P3 – P8 are not used by the DCE-1400 and must be left at their factory default setting. All ten switches are set to the open position and each jumper connects the center post with the post near its Px silkscreen.

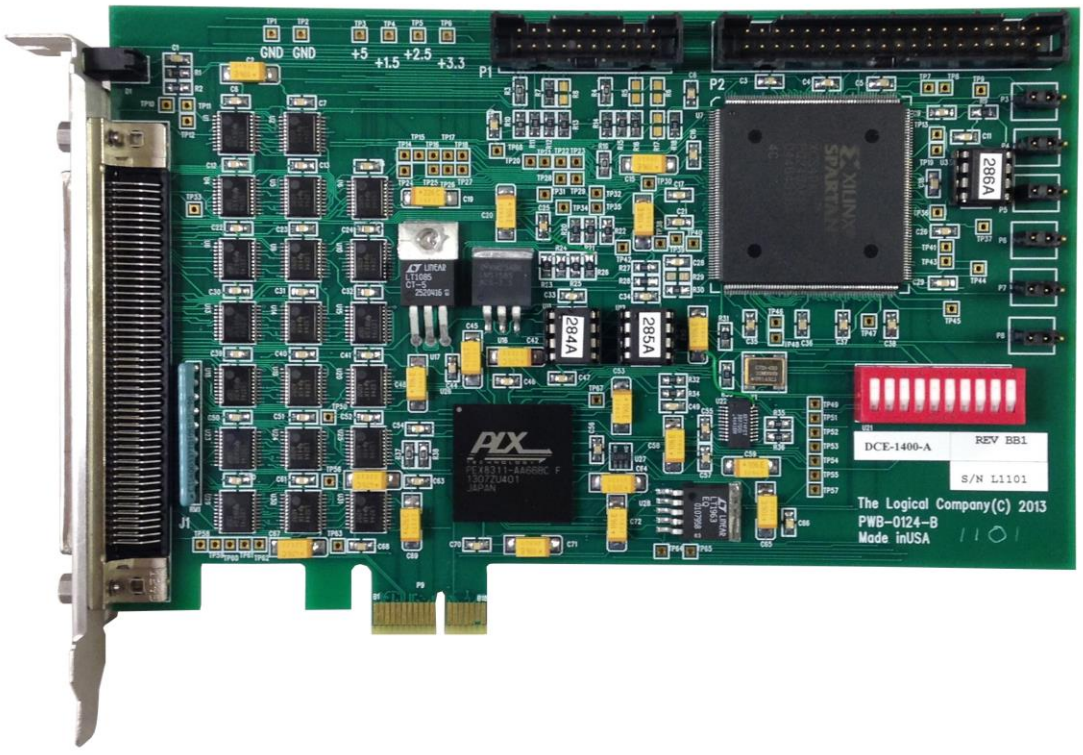



Figure 1-1: DCE-1400 Module

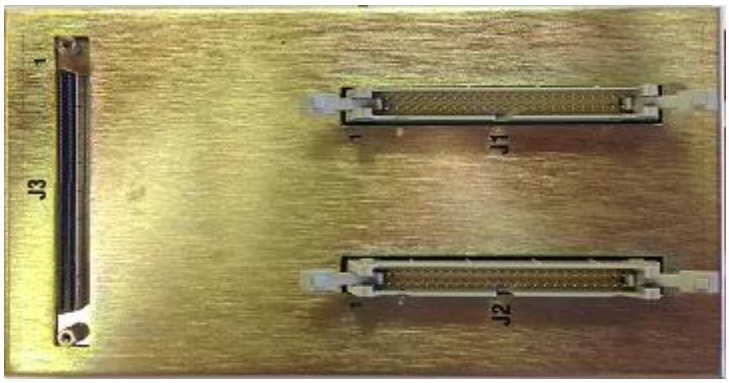



Figure 1-2:  CPX-1403 Panel

# 1. Open the workstation enclosure or expansion chassis

To remove the cover from the workstation or expansion chassis enclosure:

A. Shut down the system software as described in the instructions that came with your software.

B. Remove power to the system unit or expansion chassis.

C. Open the enclosure as described in the manuals that came with the unit.

**Note**

Use the anti-static wrist strap supplied with your system unit to prevent damage to the equipment. Clip the free end of the strap to the metal frame of the enclosure.

# 2. Install the DCE-1400 controller.

A. Refer to the manual that came with the system to install the DCE-1400 controller in any available full height, half length PCIe slot.

B. Make sure that DCE-1400 controller does not make contact to a heath sink or other component(s) and it is firmly seated and mechanically secured.

C. Replace the cover on the enclosure and secure it.

# 3. Cable the controller to the adapter panel

Use the CAB-1104-8 cable to connect J1 of the controller to connector J3 of the DCE-1400 adapter panel. The adapter panel is provided with screw slots for RETMA rack mount or wall mount. The panel also has no-mar feet for desktop or floor use.

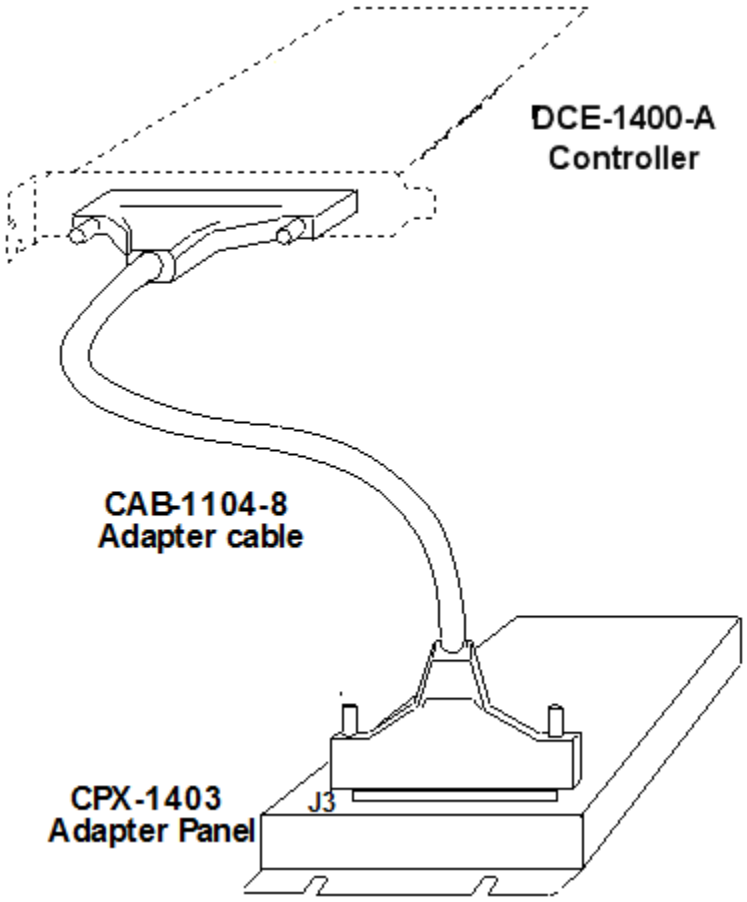



Figure 1-3: Cabling the Controller to the Adapter Panel

# 4. Cable the user equipment to the adapter panel

Cable the J1 and J2 connectors on the CPX-1403 adapter panel to your DRV11-J compatible user equipment. Align the triangle on the cable connector with the triangle of the panel connector. See Figure 1-4.

Pin assignments for the connectors are listed in Appendix A.

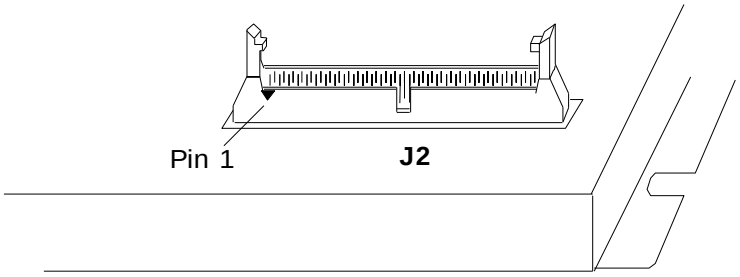



Figure 1-4: CPX-1403 User Connector

# 5. Power up the system and verify installation.

A. Apply power to the computer system and wait for booting to complete.

B. Refer to the driver manual that came with the device for driver installation and verification that the DCE-1400 is recognized by the system.

C. The DCE-1400 is supplied with a loopback cable (CAB-1402-12) to allow you to run the loopback diagnostics supplied with all DCE-1400 device drivers. Refer to the owner's manual supplied with the driver for information on the installation and operation of the diagnostic. Loopback cable CAB-1402-12 must be installed from J1 to J2 when running the diagnostic. **Note that cable is built to install with a 180 degree twist.**

# 2 General Description

## Product Description

The DCE-1400 is a parallel line interface module designed for use in workstations and servers supporting the PCIe Local bus. It takes advantage of today's FPGA technology to emulate the functionality of DEC's DRV11-J parallel line interface module. The DCE-1400 contains four programmable ports designated A, B, C and D. Each port contains sixteen I/O lines and is capable of transferring a 16-bit word between the PCIe bus and the user device(s). Data word transfers in or out of the DCE-1400 are accomplished by the assertion of two control signals at each port of the DCE-1400 and two control signals asserted by the user device to its respective port. These control signals must be asserted in a protocol sequence while observing timing constraints to ensure an orderly data transfer. The protocol sequence is described in Chapter 3.

The DCE-1400 will also accept interrupt requests from up to sixteen I/O lines. This interrupt capability makes it useful for sensor I/O applications.

The DCE-1400 may also be used as a general purpose parallel interface to custom devices or DCE-1400s may be connected together as a simple link between platforms.

The DCE-1400 contains two programmable mode registers that provide a number of operating modes to customize the module configuration for different system applications. The module may be programmed for use in vectored-interrupt-driven systems or software-polled systems. When used in vectored interrupt systems, the module may be programmed to operate in either a fixed or rotating priority mode with a single common or individual vectors in response to user device(s) interrupt requests. Additional operating options available under program control include the selection of an active high or active low interrupt request polarity, pre-selection of internal registers, and the selection of a master mask bit to arm or disarm the interrupt capability of the DCE-1400. All of the operating modes and options are described in detail in Chapter 3.

The DCE-1400 also contains an 8-bit RAM used to store programmed interrupt vectors. One vector may be programmed for each of the 16 interrupt request inputs.

# Features

- Four 3-state, 16-bit parallel I/O ports
- Acceptance of up to 16 external interrupt requests
- Program-controlled input/output operations
- Programmable operating modes:
  Interrupt Controller Mode - Interrupt-driven or polled
  Priority Modes - Fixed or Rotating

# Specifications

## Physical Dimensions

| | |
|---|---|
| DCE-1400-A Controller | Full height, half length, x1 card<br>measuring 4.376 inches by 6.60 inches<br>(11.515 cm by 16.765 cm). |
| CPX-1403 Panel | 8.75 inches by 4.00 inches by 1.00 inches<br>(22.225 cm by 10.16 cm by 2.54 cm) |

## Interface

| | |
|---|---|
| Controller to Panel: | 100-pin high density connector |
| Adapter Cable: | 8-foot, terminated with a 100-pin connector at each end. |
| Adapter Panel: | 2 50-pin DRV11-J style connectors |

## Electrical

Power Required:

| | |
|---|---|
| +3.3 volts | 0.4 amp, max |
| +12 volts | 1.0 amp, max |
| +3.3 volts aux | not used |

Bus Loading 2 ac loads, 1 dc load

I/O Signal Parameters:

Data Buffer 3-State Outputs

V(OL) = 0.5V @ I(OL) = 8mA
V(OL) = 0.4V @ I(OL) = 4mA
V(OH) = 2.4V @ I(OH) = -2.6mA

Data Buffer Inputs

I(IL) = -0.2mA @ V(IL) = 0.4V
V(IH) = 20µA @ V(IH) = 2.7V

Protocol Signal 3-State Outputs

V(OL) - 0.55V @ I(OL) = 64mA
V(OH) - 2.4V @ I(OH) = -15mA

Protocol Signal Inputs

Termination = 120Ω
I(IL) = -27mA @ V(IL) = 0.5V
I(IH) = 80µA @ V(IH) = 2.7V

## PCI Express Bus

| | |
|---|---|
| Lane Size: | x1 |
| Compliance: | 3.0 |

## Environmental

| | |
|---|---|
| Operating Conditions: | |
| Temperature | 5° to 50° C (41° to 122° F) |
| Relative Humidity | 20% to 80% noncondensing |
| Storage Conditions: | |
| Temperature | -40° to 66° C (-40° to 150° F) |
| Relative Humidity | 10% to 95% noncondensing |

# 3 Functional Description

## General Description

The DCE-1400 contains the logic necessary to provide communication between the PCIe bus and up to four user devices in 16-bit word lengths via four I/O ports. Four control lines associated with each of the four ports ensure orderly information transfers. Word transfers are executed by programmed I/O operations or interrupt-driven routines. Write data is output by the DCE-1400 to the I/O bus through 3-state data latches, and read data is input through unlatched bus buffers.

All control/status and I/O data transfers take place over a bi-directional internal bus on the DCE-1400. The module contains four I/O buses, one for each port (A, B, C and D). Each port has an associated control/status register (CSRA, CSRB, CSRC or CSRD) that contains status information when read and command words when written. All ports have 16 bi-directional 3-state lines and perform controlled input/output operations. Note that port A is the only port that will perform bit interrupt functions in addition to input/output data transfers. The 16 external interrupt requests are functionally divided into two groups of eight lines, referred to as group 1 and group 2.

## Control/Status Registers

The control/status registers (CSRA, CSRB, CSRC and CSRD) are read/write word-addressable registers with bit assignments as shown in Figures 3-1 through 3-4. The function and description of the control/status register bits are described in Tables 3-1 through 3-4.

## Control/Status Register A (CSRA)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY A | RPLY A | | | | W1 SEL | IE | DIR A | C/S 7 | C/S 6 | C/S 5 | C/S 4 | C/S 3 | C/S 2 | C/S 1 | C/S 0 |

Figure 3-1: Control/Status Register A Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | C/S 7 - C/S 0 | Read/Write | CSR A bits 07-00. These bits are used in conjunction with CSR B bits 07-00 to program interrupt control group 1. They contain status information when read and command words when written. Unaffected by PCIe RST. |
| 08 | DIR A | Read/Write | Direction A. Used for controlling DBRA. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCE-1400 RDY output signal is asserted and the DCE-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCE-1400 is the output device. The negation of either DIR or USER RDY causes the DCE-1400 outputs to remain in their high impedance state. Cleared by PCIe RST. |
| 09 | IE | Read/Write | Interrupt Enable. Enables the DCE-1400 to generate processor interrupts when set. Used to enable both group 1 and group 2 interrupts. Cleared by PCIe RST. |
| 10 | W1 SEL | Read/Write | W1 Select. Selects either USER RPLY (A-D) or A I/O (bits 15-12). When this bit is 0, USER RPLY signals are selected as interrupt sources. Cleared by PCIe RST. |
| 13-11 | NU | | Not used. Read as all zeroes. |
| 14 | RPLY A | Read Only | DCE-1400 Reply. This bit reflects the state of DCE-1400 RPLY Signal. When asserted, this bit indicates that the DCE-1400 is transferring data on the I/O port. Cleared by PCIe RST. |
| 15 | RDY A | Read only | User Ready A. Used to control DBRA. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCE-1400 output operations. The user device asserts this signal when it desires the DCE-1400 to output data. Unaffected by PCIe RST. |

Table 3-1: CSRA Bit Functions and Descriptions

## Control/Status Register B (CSRB)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY B | RPLY B | | | | | | DIR B | D 7 | D 6 | D 5 | D 4 | D 3 | D2 | D 1 | D0 |

Figure 3-2: Control/Status Register B Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | D 7 - D 0 | Read/Write | CSR B bits 07-00. These bits are used in conjunction with CSR A bits 07-00 to program interrupt control group 1. They contain information selected by the command word loaded through CSRA. The registers available are the IRR, ISR, ACR, IMR and the vector memory. Unaffected by PCIe RST. |
| 08 | DIR B | Read/Write | Direction B. Used for controlling DBRB. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCE-1400 RDY output signal is asserted and the DCE-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCE-1400 is the output device. The negation of either DIR or USER RDY causes the DCE-1400 outputs to remain in their high impedance state. Cleared by PCIe RST. |
| 13-09 | NU | | Not used. Read as all zeroes. |
| 14 | RPLY B | Read Only | DCE-1400 Reply. This bit reflects the state of DCE-1400 RPLY Signal. When asserted, this bit indicates that the DCE-1400 is transferring data on the I/O port. Cleared by PCIeRST. |
| 15 | RDY B | Read only | User Ready B. Used to control DBRB. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCE-1400 output operations. The user device asserts this signal when it desires the DCE-1400 to output data. Unaffected by PCIe RST. |

Table 3-2: CSRB Bit Functions and Descriptions

## Control/Status Register C (CSRC)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY C | RPLY C | | | | | | DIR C | C/S 7 | C/S 6 | C/S 5 | C/S 4 | C/S 3 | C/S 2 | C/S 1 | C/S 0 |

Figure 3-3: Control/Status Register C Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | C/S 7 - C/S 0 | Read/Write | CSR C bits 07-00. These bits are used in conjunction with CSR D bits 07-00 to program interrupt control group 1. They contain status information when read and command words when written. Unaffected by PCIe RST. |
| 08 | DIR C | Read/Write | Direction C. Used for controlling DBRC. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCE-1400 RDY output signal is asserted and the DCE-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCE-1400 is the output device. The negation of either DIR or USER RDY causes the DCE-1400 outputs to remain in their high impedance state. Cleared by PCIe RST. |
| 13-09 | NU | | Not used. Read as all zeroes. |
| 14 | RPLY C | Read Only | DCE-1400 Reply. This bit reflects the state of DCE-1400 RPLY Signal. When asserted, this bit indicates that the DCE-1400 is transferring data on the I/O port. Cleared by PCIe RST. |
| 15 | RDY C | Read only | User Ready C. Used to control DBRC. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCE-1400 output operations. The user device asserts this signals when it desires the DCE-1400 to output data. Unaffected by PCIe RST. |

Table 3-3: CSRC Bit Functions and Descriptions

## Control/Status Register D (CSRD)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RDY D | RPLY D | | | | | | DIR D | D 7 | D 6 | D 5 | D 4 | D 3 | D2 | D 1 | D0 |

Figure 3-4: Control/Status Register D Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07-00 | D 7 - D 0 | Read/Write | CSR D bits 07-00. These bits are used in conjunction with CSR C bits 07-00 to program interrupt control group 2. They contain information selected by the command word loaded through CSRC. The registers available are the IRR, ISR, ACR, IMR and the vector memory. Unaffected by PCIe RST. |
| 08 | DIR D | Read/Write | Direction D. Used for controlling DBRD. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DCE-1400 RDY output signal is asserted and the DCE-1400 is the input device. When this bit is set and the USER RDY signal is asserted, the DCE-1400 is the output device. The negation of either DIR or USER RDY causes the DCE-1400 outputs to remain in their high impedance state. Cleared by PCIe RST. |
| 13-09 | NU | | Not used. Read as all zeroes. |
| 14 | RPLY D | Read Only | DCE-1400 Reply. This bit reflects the state of DCE-1400 RPLY Signal. When asserted, this bit indicates that the DCE-1400 is transferring data on the I/O port. Cleared by PCIe RST. |
| 15 | RDY D | Read only | User Ready D. Used to control DBRD. When read, this bit yields the state of the USER RDY signal. A 0 means negated and a 1 means asserted. This bit is used in conjunction with the DIR bit to enable DCE-1400 output operations. The user device asserts this signal when it desires the DCE-1400 to output data. Unaffected by PCIe RST. |

Table 3-4: CSRD Bit Functions and Descriptions

# Data Buffer Registers

The four data buffer registers (DBRA, DBRB, DBRC and DBRD) are 16-bit word-addressable registers. They are used as latched output data buffers when the DCE-1400 is in output mode (write) and as unlatched bus buffers in input mode (read). The contents of an output data buffer may be examined, when in output mode and the user cables are connected to powered external equipment, by performing a read operation of the register. This ability to examine the output data buffers in the output mode provides software access to the last written data.

The latched output data buffer registers DBRA through DBRD are not cleared by PCIe RST. The bit assignment is the same for all registers and is shown in Figure 3-5.

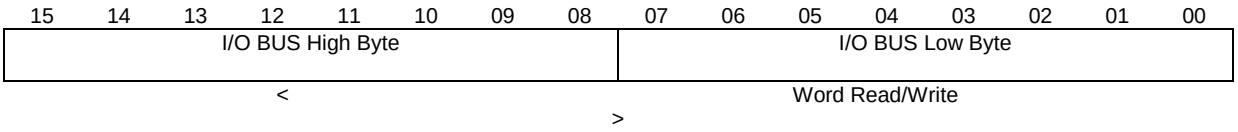



Figure 3-5: Data Buffer Register Bit Assignments

# Vector Service Register

The vector service register is read to initiate an interrupt acknowledge sequence when the DCE-1400 is programmed to operate with interrupt-driven routines. The vector can be encoded by the programmer to reflect which group and level requires service. This is particularly useful when the auto clear function is used.

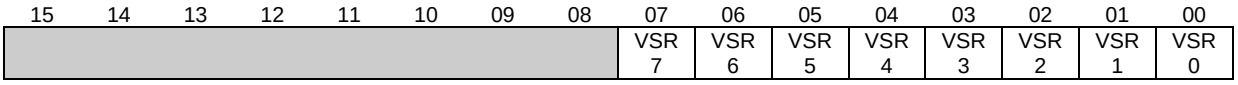



Figure 3-6: Vector Service Register

| Bit | Name | Function | Description |
|---|---|---|---|
| 15-08 | NU | | Not used. |
| 07-00 | VSR7-VSR0 | Read Only. | Vector service register bits 7-0. |

Table 3-5: Vector Service Register Bit Functions and Descriptions

# Interrupt Control

The DCE-1400 is capable of monitoring 16 lines to generate 16 interrupts. Functional and operating descriptions of the signals required to initiate interrupts and the DCE-1400 registers used for programming are provided in the sections below.

## Functional Description

There are two interrupt controllers on the DCE-1400. Each controller is responsible for monitoring a group of eight interrupt request inputs. Each group of eight interrupt requests is applied to an 8-bit interrupt request register (IRR) in the interrupt controller.

The two interrupt controllers (group 1 and group 2) are programmed independently. The group 1 interrupt controller is programmed through the low bytes of CSRA and CSRB while the group 2 interrupt controller is programmed through the low bytes of CSRC and CSRD. The only commonalities of the two groups are priority resolution and the interrupt enable (IE) CSRA bit 9. Both interrupt controllers must operate in the same mode, either interrupt or polled. Each interrupt controller contains an 8-bit interrupt mask register (IMR) that may be used to disable the processing of any undesired interrupt requests.

The group 1 interrupt controller has the higher priority and its enable output is connected to the enable input of group 2. Group 1 must be armed to accept interrupts with the master mask bit set in the mode register. When group 1 is armed, its enable output goes high, thus enabling group 2 interrupts. Therefore, whenever the interrupt mode is selected, group 1 must be armed, even if none of the group 1 interrupt requests are being used in order to pass the enable signal along to group 2.

Group 1 and group 2 may be programmed to respond to either an active high or an active low transition on the interrupt request lines. A bit in the interrupt request register (IRR) is set whenever the corresponding interrupt request line makes an inactive-to-active transition and meets the active pulse width requirements. Active pulse widths 270ns or greater set the corresponding IRR bit, while pulse widths of 30ns or less are ignored. Active pulse widths between 30ns and 270ns may or may not set the IRR bit.

## Interrupt Controller Interface

Each interrupt controller group accepts eight IRQ inputs. When an active interrupt, for example IRQ7, is applied to group 1, a group interrupt (GPINT) is generated if the request is not masked by the IMR. The GPINT signal generates a local interrupt (LINT) if the software has enabled interrupts by setting the interrupt enable bit and the master mask bit has not disarmed the interrupt controller. The LINT generates a PCIe interrupt request (INTA) if the software has enabled interrupts through the Interrupt Control/Status register of the PCIe interface. The PCIe interface chip must be programmed (Interrupt Control/Status bits 8 and 11) to pass the interrupt to the PCIe bus. The processor will use the PCIe interrupt vector presented by the interrupting device to pass control to the driver assigned to service that

vector. When the device driver is ready to service the DCE-1400 interrupt request it reads the Vector Service Register (VSR). On the leading edge of the VSR read, the interrupt controllers perform priority arbitration to select the highest unmasked pending interrupt and then output a vector associated with the selected interrupt request. The highest priority unmasked request is latched on the leading edge of the read so that any higher requests that may be received during the present interrupt sequence does not cause confusion and cause the wrong vector to be read.

## Interrupt Controller Operating Description

The Interrupt controllers for group 1 and group 2 are identical, except as otherwise noted, and the following description applies to both. Interrupt requests (IRQ7-IRQ0) are latched in the interrupt request register (IRR). Any requests not masked by the interrupt mask register (IMR) cause a group interrupt (GPINT) output to control logic that pass the request to the PCIe interface chip as LINT providing that the Master Mask Bit is set to the armed state and IE (CSRA) bit 9 is set. The LINT generates a PCIe interrupt request (INTA) if the software has enabled interrupts through the interrupt Control/Status register of the PCIe interface. When the processor reads the VSR the priority of pending interrupts is resolved and the associated vector is read from RAM and output onto the data bus.

Other interrupt management functions are controlled by the auto-clear register (ACR), the interrupt service register (ISR), and the mode register (MR). The command register is used by the processor to exercise control over the many functions provided by the DCE-1400 while the status register reports on the internal condition of the DCE-1400.

Each interrupt controller is addressed by the processor as either a control port or a data port. The control port provides direct access to the command register and the status register. The data port is used to communicate with all other internal locations.

The status register is selected directly for reading by the control input. Other internal registers are read by pre-selecting the desired register with mode bits 5 and 6, and then executing a data read through CSRB for group 1 and CSRD for group 2. The vector memory can be read only with a read of the vector service register during an interrupt operation.

The command register is selected directly for writing by the control input. The mask and auto-clear registers are loaded following specific commands to that effect. To load each level (IRQ7-IRQ0) of the vector memory, the vector memory pre-select command is issued to select the desired level. A data-write operation is then executed to load that level.

## Interrupt Control Reset

The reset function is accomplished by a software command, or automatically during power-up. The processor may initiate a reset at any time by writing all 0s into the command register of each interrupt controller (CSRA bits 7-0 for group 1, CSRC bits 7-0 for group 2). Power-up reset circuitry on each interrupt controller integrated circuit is internally triggered by the

rising $V_{CC}$ voltage (IC supply voltage 5V) to generate a brief reset pulse when the predetermined threshold is reached.

The vector memory contents are cleared by PCIe RST. Therefore, if the vector memory is to be used, it must be initialized by the processor after power-up.

The interrupt mask register is set to all 1s by either a software reset command or a power-up reset, thus disabling recognition of interrupts by the DCE-1400. The status registers continue to reflect the internal condition of group 1 and group 2 and are not otherwise affected by a reset.

The mode registers are cleared to all 0s to provide the DCE-1400 with a reasonable operating environment after a power-up or software reset command. The mode registers after reset are assigned to following options:

Interrupt mode
Individual vectoring
Fixed interrupt priority
IRQ polarity active low
ISR pre-selected for reading
Interrupt controllers disarmed by master mask bit

## Interrupt Control Register Description

The DCE-1400 uses the control and operation registers, plus the vector memories of the interrupt controllers to perform and manage its many functions. Table 3-6 lists these elements and summarizes their size and number.

| Description | Register Abbreviation | Bits Size per Register | Quantity per DCE-1400 |
|---|---|---|---|
| Interrupt request register | IRR | 8 | 2 |
| Interrupt service register | ISR | 8 | 2 |
| Interrupt mask register | IMR | 8 | 2 |
| Auto-clear register | ACR | 8 | 2 |
| Vector service register | VSR | 8 | 1 |
| Status register | - | 8 | 2 |
| Mode register | - | 8 | 2 |
| Command register | - | 8 | 2 |
| Vector memory | - | 8x8* | 16 |

*Each interrupt controller contains 8 vector memory locations of 8 bits each.

Table 3-6: Interrupt Control Register and Memory Summary

## Status Register

Each status register is eight bits wide and contains information describing the internal state of the DCE-1400. The status register is read directly by executing a read operation at CSRA for group 1 or CSRC for group 2. Figure 3-7 shows the status register bit assignments.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| S7 | S6 | S5 | S4 | S3 | S2-S0 | | |

Figure 3-7: Status Register Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07 | S7 | | Group Interrupt.<br>1 = No unmasked IRR bit set<br>0 = At least one unmasked IRR bit set<br>This bit reflects the information state of the group interrupt (GPINT) signal. Bit S7 remains valid when interrupts are disabled by the polled mode option, thus permitting the processor to check for interrupts by reading the status register. |
| 06 | S6 | | Enable Input (Group 2 only)<br>0 = Disabled<br>1= Enabled<br>This bit reflects the state of the enable-in (EI) input signal and indicates if group 2 is enabled or disabled. When S6 is high, group 2 can generate an interrupt request. When S6 is low, group 2 interrupt requests are disabled. Group 1 is always enabled. |
| 05 | S5 | | Priority Mode<br>0 = Fixed<br>1 = Rotating<br>This bit reflects the state of the priority mode option as specified by mode register bit M0. When S5 is high, rotating priority is selected. When S5 is low, fixed priority is selected. |

Table 3-7: Status Register Bit Functions

| Bit | Name | Function | Description |
|---|---|---|---|
| 04 | S4 | | Interrupt Mode<br>0 = Interrupt<br>1 = Polled<br>This bit reflects the state of the interrupt mode option as specified by mode register bit 2. When S4 is high, the polled mode is selected and interrupt requests are disabled. When S4 is low, the interrupt mode is selected. |
| 03 | S3 | | Master Mask Bit<br>0 = Disarmed<br>1 = Armed<br>This bit reflects the state of the master mask bit as specified by mode register bit M7. When S3 is low, the group is disarmed and IRR bits that are set do not generate interrupt requests. When S3 is high, the group is armed and interrupts can occur. |
| 02-00 | S2-S0 | | For internal use only. May read as zeros or ones. |

Table 3-7: Status Register Bit Functions (cont'd)

## Command Register

Each command register is eight bits wide and is used to store the most recently entered command. The register is loaded directly from the data bus by executing a write operation at CSRA for group 1 or CSRC for group 2. Depending on the specific command opcode that is entered, an immediate internal activity may be initiated, or CSRB and CSRD may be pre-conditioned for subsequent register transfers. The opcodes for each command operation are described in the "Command Descriptions" section later in this chapter.

## Mode Register

Each mode register is eight bits wide and is used to establish the operating modes and conditions for the many functional features of the DCE-1400. The mode register allows the processor to customize the interrupt system for a particular application. Figure 3-8 shows the mode register bit assignments. No single command or interface operation loads all bits of the mode command register. Mode bits M5, M6 and M7 are controlled by separate commands. The mode register contents cannot be read out on the data bus. However, the conditions of mode bits M0, M2 and M7, which reflect the priority, interrupt and master mask bit modes, are available as part of the status register. The mode register is cleared by a software reset command or a power-up reset.

| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|
| M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |

Figure 3-8: Mode Register Bit Assignments

| Bit | Name | Function | Description |
|---|---|---|---|
| 07 | M7 | Master Mask Bit | 0 = Disarmed<br>1 = Armed |
| 06-05 | M6-M5 | | Register Pre-selection<br>00 = Interrupt service<br>01 = Interrupt mask<br>10 = Interrupt request register<br>11 = Auto clear register |
| 04 | M4 | | Ireq Polarity<br>0 = Active low<br>1 = Active High |
| 03 | M3 | | Unused. Must be 0. |
| 02 | M2 | | Interrupt mode<br>0 = Interrupt<br>1 = Polled |
| 01 | M1 | | Vector Selection<br>0 = Individual vector<br>1 = Common vector |
| 00 | M0 | | Priority Mode.<br>0 = Fixed<br>1 = Rotating |

Table 3-8: Mode Register Bit Functions

**Interrupt Request Register (IRR)**

Each IRR is eight bits wide and is used to recognize and store active transitions on the eight interrupt request lines. A bit in the IRR is set whenever the corresponding IRQ input line makes an inactive-to-active transition and meets the minimum active pulse width requirements. Also, the processor (under program control) may set the IRR bits by using two types of commands. This capability permits software-initiated interrupts and is a useful tool for system testing.

All IRR bits are cleared by a reset. Individual IRR bits are cleared automatically when their interrupts are acknowledged by the processor. Four types of commands, in addition to reset, allow the processor to clear IRR bits.

The IRR may be read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CSRB bits 7-0 for group 1 or CSRD bits 7-0 for group 2.

**Interrupt Service Register (ISR)**

Each ISR is eight bits wide and is used to store the acknowledge status of individual interrupts. When the processor acknowledges an interrupt request, the DCE-1400 selects the highest priority request that is pending, clears the associated IRR bit, and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing, it is reset by the internal hardware before the end of the acknowledge sequence. When the ISR bit is not programmed for automatic clearing, it must be reset by command from the processor.

The DCE-1400 uses the ISR internally to erect a "masking fence." When an ISR bit is set and fixed priority mode is selected, only requests of higher priority causes a new group interrupt (GPINT) output. Thus, requests from lower priority interrupts (and from new requests associated with the set ISR bit) will be "fenced out" and ignored until the ISR bit is cleared. In the rotating priority mode, all requests are fenced out by an ISR bit that is set and no new interrupts are generated until the ISR bit is cleared. When automatic clearing is specified, no masking fence is erected since the ISR bit is cleared.

When in the fixed mode, if an unmasked interrupt arrives from a device of higher priority than the current ISR, the processor will be interrupted if its interrupt input is enabled. When the new interrupt is acknowledged, the associated higher priority ISR bit is set and the fence moves up to the new priority level. When the new ISR bit is cleared, the fence will then fall back to the previous ISR level. The ISR may be read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CSRB (bits 7-0) for group 1 or CSRD (bits 7-0) for group 2.

**Interrupt Mask Register (IMR)**

Each IMR is eight bits wide and is used to enable/disable the processing of individual interrupts. Only unmasked IRR bits can generate an interrupt. The IMR does not otherwise affect the operation of the IRR. An IRR bit that is set while masked will cause an interrupt when its IMR bit is cleared.

All eight IMR bits for each group may be set, cleared, read or loaded in parallel by the processor. In addition, individual IMR bits may be set or cleared by command. This allows a control routine to enable or disable directly an individual interrupt without disturbing the other mask bits and without knowledge of their state or context.

The IMR polarity is active high for masking: a 0 enables the interrupt and a 1 disables it. The power-on reset and the software reset command cause all IMR bits to be set, thus disabling

all interrupt requests. The IMR may be read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CSRB (bits 7-0) for group 1 or CSRD (bits 7-0) for group 2.

**Auto-Clear Register (ACR)**

Each ACR is eight bits wide and specifies the automatic clearing option for each of the ISR bits. When an auto-clear bit is set, the corresponding ISR bit set in an interrupt acknowledge cycle (VSR read) is cleared by the internal hardware before the end of the sequence. When an auto-clear bit is not set, the corresponding ISR bit that has been set by VSR read is cleared by a command from the processor.

When selected, the auto-clear option provides two related functional effects. First, it eliminates the need for the associated interrupt service routine to issue a command to clear the ISR bit. Second, it eliminates the masking fence that would otherwise have been erected, allowing lower priority interrupts to cause a new interrupt request.

The ACR is loaded in parallel from the data bus by issuing the ACR load pre-select command, followed by a write into the data port. The ACR is read onto the data bus by pre-selecting it in mode register bits M5 and M6 with a load mode register command, followed by a read of CRSB (bits 7-0) for group 1 or CSRD (bits 7-0) for group 2.

**Vector Memory**

The vectors are programmed by the vector memory pre-select command, followed by a data-write operation to load the vector required for each interrupt request level. The vector memory pre-select command is entered directly into the low byte (bits 7-0) of CSRA for group 1 or the low byte (bits 7-0) of CSRC for group 2. Pre-select commands entered through CSRA select CSRB for subsequent loading of the vectors in group 1. Pre-select commands entered through CSRC select CSRD to load the addresses for group 2.

One vector is loaded after each pre-selection command. Vectors are read through the Vector Service Register by a device driver during an interrupt service operation.

Loading a vector into each new interrupt request level must be preceded by a new vector memory pre-select command. Therefore, 16 pre-select commands, each followed by a data-write operation, are required to load 16 vectors into the vector memory.

The DCE-1400 only uses one vector per interrupt. To ensure proper operation, load only one data value after each pre-select command.

# Operating Options

The mode register bits are program-controlled to establish the combination of interrupt operating options desired for a particular DCE-1400 system applications. Refer to Figure 3-8 for the mode register bit assignments. A detailed description of the various options available follows. The master mask bit affects both group 1 and group 2; all other mode bits affect only their corresponding groups.

### Interrupt Priority Mode Selection

Mode register bit M0 specifies either a fixed or rotating resolution mode for the DCE-1400. When M0 is low, fixed priority is selected and the eight IRQ inputs for both group 1 and group 2 are assigned a priority based on their physical location at the interface. Group 1 IRQ 0 has the highest priority and group 2 IRQ 7 has the lowest. Table 3-9 lists the priority assigned to the A I/O (bits 15-0) lines and the USER RPLY lines.

| Group | Connection | Level | IRR,ISR,IMR,ACR Bit Assignments | | Priority |
|---|---|---|---|---|---|
| 1 | A I/O 0 | 0 | D0 | | Highest |
| 1 | A I/O 1 | 1 | D1 | | |
| 1 | A I/O 2 | 2 | D2 | | |
| 1 | A I/O 3 | 3 | D3 | CSRB | |
| 1 | A I/O 4 | 4 | D4 | | |
| 1 | A I/O 5 | 5 | D5 | | |
| 1 | A I/O 6 | 6 | D6 | | |
| 1 | A I/O 7 | 7 | D7 | | |
| 2 | A I/O 8 | 0 | D0 | | |
| 2 | A I/O 9 | 1 | D1 | | |
| 2 | A I/O 10 | 2 | D2 | | |
| 2 | A I/O 11 | 3 | D3 | CSRD | |
| 2 | USER RPLY A | 4* | D4 | | |
| 2 | USER RPLY B | 5* | D5 | | |
| 2 | USER RPLY C | 6* | D6 | | |
| 2 | USER RPLY D | 7* | D7 | | Lowest |

* W1SEL (CSRA bit 10) selects either USER RPLY A-D (W1SEL=0) or A I/O 15-12 (W1SEL=1).

Table 3-9: Fixed Priority Mode

Interrupt acknowledge operations are initiated by the processor in response to a PCIe (INTA) interrupt output.

Interrupt priority is resolved after the processor initiates the interrupt acknowledge sequence. When the processor reads the Vector Service Register, the interrupt controllers perform priority arbitration to select the highest unmasked pending interrupt, and then output a vector associated with the selected interrupt request. In the fixed priority mode, therefore, devices with a high priority may be serviced many times before a lower priority device is serviced once. In many systems, this is an appropriate method of servicing the interrupting devices. In those systems where this is not an appropriate method, the interrupt masking capability of

the DCE-1400 may be used to modify the effective priority structure. This may be accomplished by masking out recently serviced high priority devices, thus permitting recognition of lower priority inputs.

Alternatively, the rotating priority mode may be selected for use in systems where the eight interrupts of each group have similar priority and bandwidth requirements. Mode register bit M0=1 selects the rotating priority mode. As shown in Figure 3-9, the relative priorities remain the same as in the fixed mode. In the rotating priority mode, however, the lowest priority position in the circular chain is assigned by the hardware to the most recently serviced interrupt. Priority rotation occurs only within a given group and priority between group 1 and group 2 remains fixed, with group 1 having the higher priority.

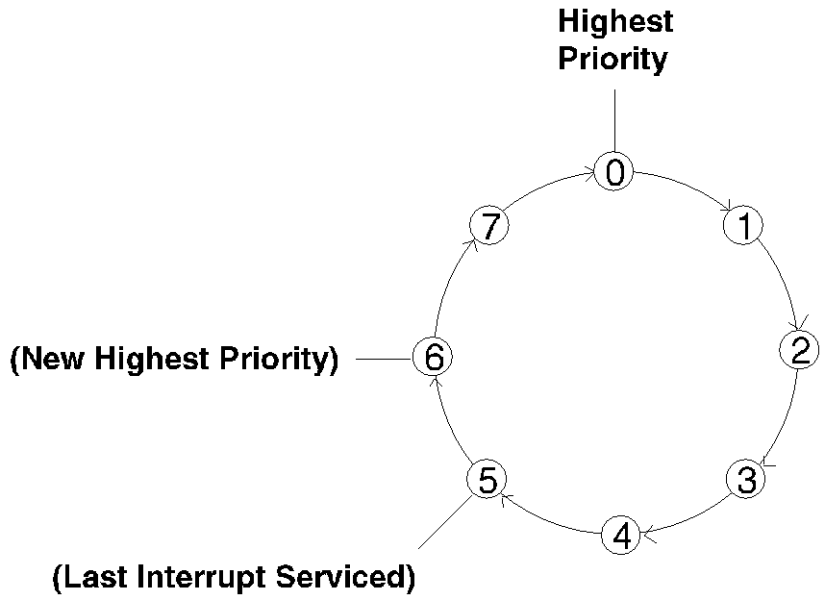



Figure 3-9: Rotating Priority Mode

The example shown in the figure assumes IRQ5 has been serviced and is assigned the lowest priority (7). IRQ 6 now occupies the new highest priority position, IRQ 7 next to the highest, etc. If two new interrupts simultaneously arrive at IRQ 1 and IRQ 4, IRQ 1 is selected and becomes the lowest priority. IRQ 4 is then acknowledged unless an active input of IRQ 2 or IRQ 3 arrives in the meantime.

This rotating scheme prevents any one interrupt request from dominating the system. An interrupt request does not have to wait for more than seven more service cycles before being acknowledged. Priority is resolved when the ISR bit of the presently selected interrupt is cleared.

In the rotating priority mode, inputs other than the one currently serviced are fenced out and will not cause interrupts until the ISR bit is cleared. Thus, only one bit at a time is set in the

ISR. Use care when selecting the rotating mode to keep from doing so again when more than one ISR is set.

### Individual Vector or Common Vector Mode

Bit M1 of the mode register specifies the vectoring option. When M1 = 0, the individual vector mode is selected and each interrupt request line is associated with its own location in the vector memory. Each location contains the vector that was loaded by the program after system power-up.

When M1 = 1, the common vector mode is selected and all vector information is supplied from the vector memory location associated with interrupt request line 0 (IRQ 0), regardless of which interrupt request line is acknowledged. The common vector mode is useful in systems where several similar devices share a common service routine and direct individual device identification is not important. This may be true because of the nature of the peripheral-system interaction or in the case of a transient system condition that uses the common vector temporarily to save the additional programming overhead required to load the vector memory twice per group.

### Interrupt or Polled (Flag) Mode

Bit 2 of the mode register allows the system to enable or disable interrupt requests. When M2 = 0, the interrupt mode is selected and interrupts are enabled. The interrupt mode may be considered the “normal” mode because it permits full use of the interrupt control and management capabilities of the DCE-1400.

When M2 = 1, the polled mode is selected, which forces the group interrupt (GPINT) output of the interrupt controllers to the inactive state and thus prevents the DCE-1400 from issuing a bus interrupt request. Since no bus interrupt requests are supplied, the processor cannot initiate the interrupt acknowledge sequence. Consequently, ISR bits are not set, masking fences are not erected, and IRR bits are not automatically cleared. Polled-mode operation requires the software to read the status register to determine if requests are pending. Software routines must then be used to determine which input line requested the interrupt. IRR bits may be cleared by the software. The polled mode of operation effectively bypasses the hardware interrupt, vectoring, and fencing functions of the DCE-1400. What remains is the interrupt request latching and masking functions.

### Mode Register Bit 3

Bit 3 of the mode register is not used.

### IRQ Polarity Option

Bit 4 of the mode register specifies the polarity of interrupt request inputs to which the DCE-1400 will respond. When M4 = 0, the interrupt request inputs are selected as active low and

a negative-going transition is required to set the associated IRR bits. When M4 = 1, the interrupt request inputs are selected as active high and a positive-going transition is required to set the associated IRR bits. This polarity option may be used to simplify the design of the DCE-1400 interface to the interrupting devices.

### Register Pre-selection Option

Bits 5 and 6 of the mode register specify the internal data register contents that will be output by the DCE-1400 during a read operation at the data port. These bits do not affect destinations for write operations. The four registers that may be read are the IRR, ISR, IMR and ACR. Pre-select coding for each register is shown in Figure 3-8. The pre-selection remains in effect for all data transfers until the contents of M5 and M6 are changed.

The ability to examine these operating registers in conjunction with the status register contents provides important information regarding the current internal conditions of the DCE-1400. The processor's access to these registers permits dynamic operating flexibility and provides important diagnostic, testing, and debugging information.

### Master Mask Option

Bit 7 of the mode register specifies the armed status of the DCE-1400 by way of the master mask control bit. When M7 = 0, the group is disarmed as if all eight bits in the IMR had been set. IRQ inputs are accepted and latched but are treated as if masked. When M7 = 1, the group is armed and any active unmasked interrupt inputs may cause interrupt requests to the processor.

The master mask option permits the system to disarm a group and prevent the processing of interrupts without disturbing the contents of the IMR. Thus, when the group is re-armed, the old IMR conditions are still valid and need not be reloaded. Note that a single command to the master mask bit of the highest priority interrupt group (Group 1) shuts down the entire interrupt system. This is the only mode bit that affects both groups.

## System Operating Sequence

The management of interrupts by the DCE-1400 requires interaction between the processor, the DCE-1400, and the user device. The operations performed by the system are described in the following typical sequence of events. The DCE-1400 is initialized, enabled, and ready to run in the interrupt mode. The processor has enabled its internal interrupt structure to accept DCE-1400 interrupt requests.

1. One (or more) of the IRQ inputs becomes active, indicating that service is desired.

2. The requests are captured and latched in the IRR. The latching action of the IRR cannot be disabled and active requests are always stored unless a previous request at the same IRR bit has not been cleared.

3. If the active IRR bit is masked by the corresponding bit in the IMR, no further action takes place. When the IRR bit is not masked, an interrupt request is generated.

4. When the processor recognizes an interrupt request, it completes the execution of its current instruction and then executes an interrupt acknowledge cycle.

5. When the VSR is read, the DCE-1400 begins selection of the highest priority unmasked IRR bit. All interrupts that have become active before the leading edge of the VSR read are considered for selection. When selection is complete, the contents of the vector memory location associated with the selected request are accessed.

6. In parallel with the transfer of the vector, the DCE-1400 automatically clears the selected IRR bit and sets the selected ISR bit. If the auto-clear function is not in force for the selected interrupt, the ISR bit causes the erection of a masking fence, and interrupts are disabled until a higher priority interrupt arrives (if in fixed priority mode) or until the ISR bit is cleared. The interrupt service routine must clear the ISR bit near the end of the routine if the auto-clear function is not used.

7. If a higher priority request arrives while the current request is being serviced, and if the fixed priority mode is in effect, the DCE-1400 outputs another interrupt request (nested interrupt). The processor recognizes the interrupt signal only if it has enabled its internal interrupt logic. If this new request is acknowledged, the DCE-1400 clears the corresponding IRR bit and sets the ISR bit.

8. When the processor has completed all service associated with the interrupt, it clears the remaining ISR bit (if the auto-clear capability is not used), enables its internal interrupt system (if it has not already done so), and returns to the main program.

# Command Descriptions

The DCE-1400 command set allows the processor to customize the interrupt operating modes and options for a particular application. Commands are also used to initialize and update the vector memory locations and to manipulate the internal controlling bits set during interrupt servicing. Commands are entered directly into the command register by writing into the low byte of CSRA for group 1 or CSRC for group 2. Pre-selection commands entered through CSRA select CSRB for subsequent group 1 register transfers. Pre-selection commands entered through CSRC select CSRD for subsequent group 2 register transfers. All the available commands are described below and are summarized in Table 3-10. An “X” in any bit position of the command code indicates a “don’t care” condition. Any commands that alter the state of the IMR, IRR or master mask bit should be executed with the processor status word at a priority level equal to the DCE-1400 to prevent undefined interrupts from occurring.

| Command Code | | | | | | | | Command Description |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | 1 | 0 | X | X | X | Clear all IRR and IMR bits. |
| 0 | 0 | 0 | 1 | 1 | B2 | B1 | B0 | Clear the IRR and IMR bits specified by the B2, B1, B0 field. |
| 0 | 0 | 1 | 0 | 0 | X | X | X | Clear all IMR bits. |
| 0 | 0 | 1 | 0 | 1 | B2 | B1 | B0 | Clear the IMR bit specified by the B2, B1, B0 field. |
| 0 | 0 | 1 | 1 | 0 | X | X | X | Set all IMR bits. |
| 0 | 0 | 1 | 1 | 1 | B2 | B1 | B0 | Set the IMR bit specified by the B2, B1, B0 field. |
| 0 | 1 | 0 | 0 | 0 | X | X | X | Clear all IRR bits. |
| 0 | 1 | 0 | 0 | 1 | B2 | B1 | B0 | Clear the IRR bit specified by the B2, B1, B0 field. |
| 0 | 1 | 0 | 1 | 0 | X | X | X | Set all IRR bits. |
| 0 | 1 | 0 | 1 | 1 | B2 | B1 | B0 | Set the IRR bit specified by the B2, B1, B0 field. |
| 0 | 1 | 1 | 0 | X | X | X | X | Clear the highest priority ISR bit. |
| 0 | 1 | 1 | 1 | 0 | X | X | X | Clear all ISR bits. |
| 0 | 1 | 1 | 1 | 1 | B2 | B1 | B0 | Clear the ISR bit specified by the B2, B1, B0 field. |
| 1 | 0 | 0 | M4 | M3 | M2 | M1 | M0 | Load mode register bits 0-4 with the specified pattern. |
| 1 | 0 | 1 | 0 | M6 | M5 | 0 | 0 | Load mode register bits 5 and 6 only, with the specified pattern. |
| 1 | 0 | 1 | 0 | M6 | M5 | 0 | 1 | Load mode register bits 5 and 6 and set mode bit 7. |
| 1 | 0 | 1 | 0 | M6 | M5 | 1 | 0 | Load mode register bits 5 and 6 and clear mode bit 7. |
| 1 | 0 | 1 | 1 | X | X | X | X | Pre-select the IMR for subsequent writing through CSRB or CSRD. |
| 1 | 1 | 0 | 0 | X | X | X | X | Pre-select the ACR for subsequent writing through CSRB or CSRD. |
| 1 | 1 | 1 | X | X | L2 | L1 | L0 | Pre-select the vector memory request level specified by the L2, L1, L0 field for subsequent writing through CSRB or CSRD. |

Note: X = “don’t care” condition

Table 3-10: DCE-1400 Command Code Summary

## Reset

The reset command allows the processor to establish a known internal condition. The vector memory and byte count register are not affected by the software reset. The IMR is set to all 1s. The ISR, IRR, ACR and mode registers are cleared to all 0s.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Clear IRR and IMR

All bits in the IMR and IRR are cleared at the same time. Thus, all interrupts are enabled and the previous history of all IRQ transitions is forgotten. If the interrupt request is active when the command is entered, it becomes inactive.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | X | X | X |

## Clear Single IMR and IRR Bit

The same single bit is cleared in both the IMR and IRR. Other bits are not changed. If the specified IRR bit is generating an active interrupt output, the interrupt request may become inactive upon entry of the command. The bit position cleared is specified by the B2, B1, B0 field as shown in Table 3-11.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | B2 | B1 | B0 |

| **Command Register Field** | | | **Bit Specified** |
|---|---|---|---|
| **B2** | **B1** | **B0** | |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

Table 3-11: Command Register B2, B1, B0 Field Coding

### Clear IMR

All bits in the IMR are cleared. All IRR bits are therefore unmasked and any IRR bits that are set cause an active interrupt request after the command is entered.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | X | X | X |

### Clear Single IMR Bit

A single bit in the IMR is cleared. Other bits are not changed. If the corresponding bit in the IRR is set, it is unmasked and can cause an active interrupt request after entry of the command. The IMR bit cleared is specified by the B2, B1, B0 field as shown in Table 3-11.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | B2 | B1 | B0 |

### Set IMR

All bits in the IMR are set to 1. All IRR bits are therefore masked and unable to generate an interrupt request. If the interrupt request is active, it becomes inactive after the command is entered.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | X | X | X |

### Set Single IMR Bit

A single bit in the IMR is set. Other bits are not changed. If the corresponding bit in the IRR is active and generating an interrupt, the interrupt request becomes inactive after the command is entered. The IMR bit set is specified by the B2, B1, B0 field as shown in Table 3-11.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | B2 | B1 | B0 |

### Clear IRR

All bits in the IRR are cleared. The interrupt request becomes inactive. New transitions on the IRQ inputs are necessary to cause an interrupt.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | X | X | X |

### Clear Single IRR Bit

A single bit in the IRR is cleared, it will not cause an interrupt until it is set. The IRR bit cleared is specified by the B2, B1, B0 field as shown in Table 3-11.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | B2 | B1 | B0 |

### Set IRR

All bits in the IRR are set to 1. Any that are unmasked can cause an interrupt request. This command allows the processor to initiate eight interrupts in parallel.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | X | X | X |

### Set Single IRR Bit

A single bit in the IRR is set to 1; if unmasked, it can generate an interrupt request. This command allows the processor to simulate with software the arrival of a hardware interrupt request. It also gives the software access to the hardware priority resolution, masking, and control features of the DCE-1400. The bit set is specified by the B2, B1, B0 field as shown in Table 3-11.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | B2 | B1 | B0 |

### Clear Highest Priority ISR Bit

A single bit in the ISR is cleared. If only one bit is set, the set bit is cleared. If more than one bit is set, this command clears the bit with the highest priority. This command is useful in software contexts where the service routine does not know which device is being serviced. It should be used with caution since the highest priority ISR bit may not really be the bit intended. When using the auto-clear option on some interrupts, and/or when a subroutine nesting hierarchy is not priority-driven, the highest priority ISR bit may not correspond to the bit being serviced.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | X | X | X |

### Clear ISR

All bits in the ISR are cleared. Mask fencing is eliminated.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | X | X | X |

### Clear Single ISR Bit

A single bit in the ISR is cleared. If the bit was already cleared, no effective operation takes place. The bit cleared is specified by the B2, B1, B0 field as shown in Table 3-11. This command is most useful to service routines in managing the ISR without the help of the auto-clear option.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | B2 | B1 | B0 |

### Load Mode Bits M0 through M4

The five low-order bits of the command register are transferred into the five low-order bits of the mode register. This command controls all of the mode options except the master mask and the register pre-selection.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | M4 | 0 | M2 | M1 | M0 |

### Control Mode Bits M5, M6, and M7

The M6, M5 field in the command is loaded into the M6, M5 locations in the mode register. This field controls the register pre-selection bits in the mode register. The N1, N0 field in the command controls mode bit M7 (master mask) and is decoded as shown in Table 3-10.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | M6 | M5 | N1 | N0 |

| N1 | N0 | |
|---|---|---|
| 0 | 0 | No change to M7 |
| 0 | 1 | Set M7 |
| 1 | 0 | Clear M7 |
| 1 | 1 | (Illegal) |

Thus, this command may be considered as three distinct commands, depending on the coding of N1 and N0.

1. Load M5, M6 only.
2. Load M5, M6, and set M7.
3. Load M5, M6, and clear M7.

The command summary in Table 3-10 lists these three versions.

### Pre-select IMR for Writing

The IMR is targeted for loading from the data bus when the next write operation occurs at the data port. All subsequent data-write operations also load the IMR until a different command is entered. Read operations may be successfully inserted between the entry of this command and the subsequent writing of data into the IMR. The mode register is not affected by this command.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | X | X | X | X |

### Pre-select ACR for Writing

The ACR is targeted for loading from the data bus when the next write operation occurs at the data port. All subsequent data-write operations also load the ACR until a different command is entered. Read operations may be successfully inserted between the entry of this command and the subsequent writing of data into the ACR. The mode register is not affected by this command.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | X | X | X | X |

## Pre-select Vector Memory for Writing

One level in the vector memory is targeted for loading from the data bus by subsequent data-write operations. The L2, L1, L0 field specifies which of the eight request levels is being selected. Table 3-12 describes the IRQ-level field coding. This command should be followed by one data-write operation at CSRB group 1 or CSRD group 2 to load the desired vector. See Figure 1-3 for vector bit assignments.

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | L2 | L1 | L0 |

**IRQ Level**

| L2 | L1 | L0 | Level |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

Table 3-12: Vector Memory Field Coding

## Coding B2, B1, B0 Field Commands

Table 3-12 describes the coding of the B2, B1, B0 field of the command register that is used to set or clear a specified bit in the IRR, IMR, or ISR. Refer to Table 3-11 for a summary of the B2, B1, B0 field coding.

# 4 PCI Express Registers

## Register Description Format

The PCIe registers are contained within the ExpressLane PEX8311AA PCI Express Interface, a component produced by PLX Technology, Inc. The documentation for this component can be found on their website at, www.plxtech.com.

# 5 Programming

## General Description

The DCE-1400 may be used in systems where the data is transferred to or from the user device under program control, or in those using interrupt-driven service routines. Programmed data transfers may be performed with or without the protocol control signals (handshaking), depending on the system's complexity. The simplest of system applications may not require the handshaking signals, whereas more complicated system applications require handshaking signals to synchronize the processor with the user device.

A tutorial on programming the DCE-1400 is beyond the intended scope of this manual. However, some examples of programming the DCE-1400 can be found within the utility program, JGSET, and in the exerciser program, JGLOOP. These programs are supplied with the OpenVMS device driver, JGDRIVER, and are placed into directory [.sysmgr.jgdriver] during the device driver installation process.

# Appendix A
# User Connector Pin Assignments

Two board 50-pin male connectors (J1 and J2) interface the CPX-1403 panel to the user device. Connector J1 is used to interface the port A and port B signals, while J2 is used for the port C and port D signals. Figure A-1 shows the connector, Table A-1 lists the interface signal names and their pin numbers.

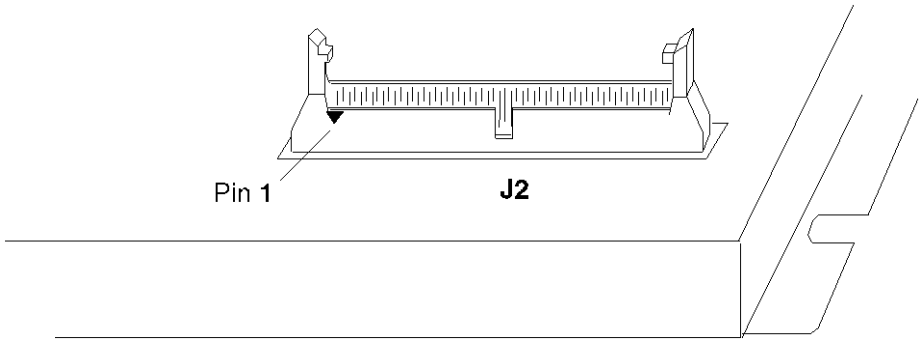



Figure A-1: CPX-1403 User Connector

| Signal Name | J1 Connector Pin | J1 Connector Pin | Signal Name |
|---|---|---|---|
| B_09 | 1 | 2 | B_12 |
| B_11 | 3 | 4 | B_08 |
| B_14 | 5 | 6 | B_15 |
| B_10 | 7 | 8 | B_13 |
| B_05 | 9 | 10 | B_07 |
| B_03 | 11 | 12 | B_01 |
| B_02 | 13 | 14 | B_00 |
| B_06 | 15 | 16 | B_04 |
| GND | 17 | 18 | B_URPLY |
| GND | 19 | 20 | B_DVRDY |
| GND | 21 | 22 | B_URDY |
| GND | 23 | 24 | B_DVRPLY |
| GND | 25 | 26 | GND |
| A_URPLY | 27 | 28 | GND |
| A_DVRDY | 29 | 30 | GND |
| A_URDY | 31 | 32 | GND |
| A_DVRPLY | 33 | 34 | GND |
| A_04 | 35 | 36 | A_06 |
| A_00 | 37 | 38 | A_02 |
| A_01 | 39 | 40 | A_03 |
| A_07 | 41 | 42 | A_05 |
| A_13 | 43 | 44 | A_10 |
| A_15 | 45 | 46 | A_14 |
| A_08 | 47 | 48 | A_11 |
| A_12 | 49 | 50 | A_09 |

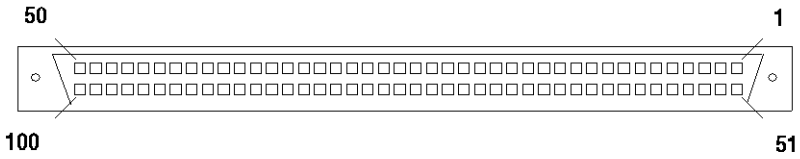
Table A-1: User Connector Pin Assignments

| Signal Name | J2 Connector Pin | J2 Connector Pin | Signal Name |
|---|---|---|---|
| C_09 | 1 | 2 | C_12 |
| C_11 | 3 | 4 | C_08 |
| C_14 | 5 | 6 | C_15 |
| C_10 | 7 | 8 | C_13 |
| C_05 | 9 | 10 | C_07 |
| C_03 | 11 | 12 | C_01 |
| C_02 | 13 | 14 | C_00 |
| C_06 | 15 | 16 | C_04 |
| GND | 17 | 18 | C_URPLY |
| GND | 19 | 20 | C_DVRDY |
| GND | 21 | 22 | C_URDY |
| GND | 23 | 24 | C_DVRPLY |
| GND | 25 | 26 | GND |
| D_URPLY | 27 | 28 | GND |
| D_DVRDY | 29 | 30 | GND |
| D_URDY | 31 | 32 | GND |
| D_DVRPLY | 33 | 34 | GND |
| D_04 | 35 | 36 | D_06 |
| D_00 | 37 | 38 | D_02 |
| D_01 | 39 | 40 | D_03 |
| D_07 | 41 | 42 | D_05 |
| D_13 | 43 | 44 | D_10 |
| D_15 | 45 | 46 | D_14 |
| D_08 | 47 | 48 | D_11 |
| D_12 | 49 | 50 | D_09 |

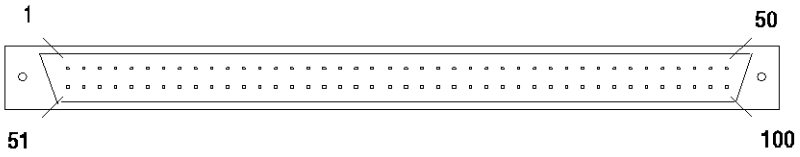
Table A-1: User Connector Pin Assignments (Cont'd)

# Appendix B
# Interconnect Cable Pin Assignments

This appendix lists the pin assignments for the interconnect cable between the DCE-1400 controller and the CPX-1403-A panel. The connectors at both ends of the interconnect cable are 100-pin high density SCSI style cable plugs. The connectors on the modules are SCSI style receptacles, AMP part number 749076-9 or Thomas & Betts Ansley part number HFR100RA29BX1. The pin assignments are listed below.




**100-pin High Density Receptacle**



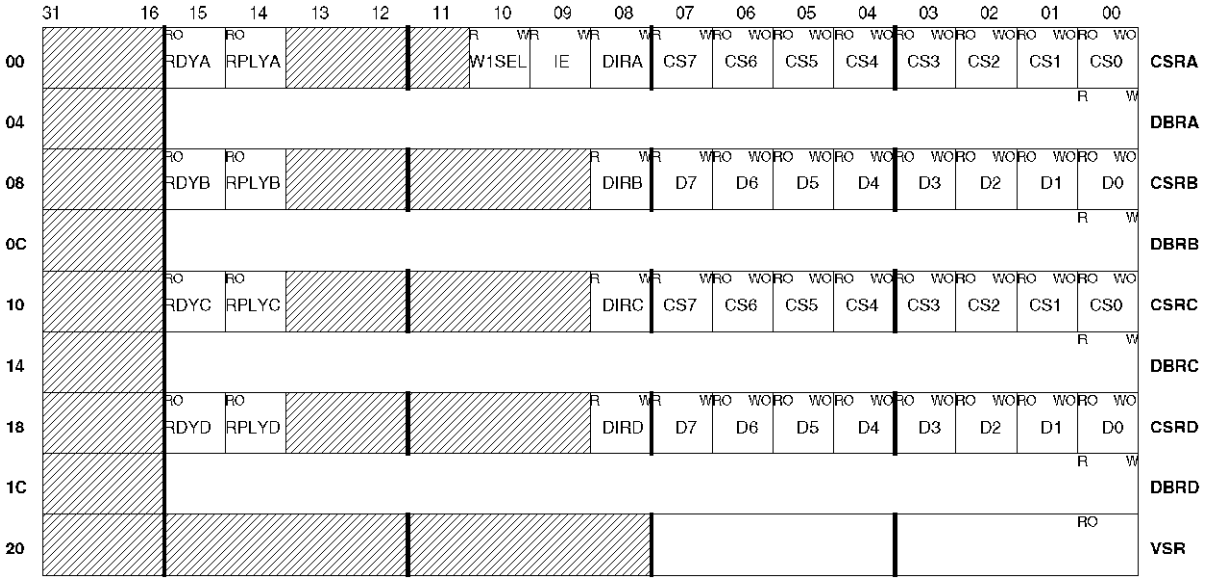

**100-pin High Density Cable Plug**

**DCE-1400 Connector J1**
**CPX-1403 Connector J3**

| Signal | Pin | Pin | Signal |
|---|---|---|---|
| GND | 1 | 51 | GND |
| A_URPLY | 2 | 52 | A_DVRPLY |
| GND | 3 | 53 | GND |
| A_URDY | 4 | 54 | A_DVRDY |
| A_08 | 5 | 55 | A_00 |
| A_09 | 6 | 56 | A_01 |
| A_10 | 7 | 57 | A_02 |
| A_11 | 8 | 58 | A_03 |
| A_12 | 9 | 59 | A_04 |
| A_13 | 10 | 60 | A_05 |
| A_14 | 11 | 61 | A_06 |
| A_15 | 12 | 62 | A_07 |
| GND | 13 | 63 | GND |
| B_URPLY | 14 | 64 | B_DVRPLY |
| GND | 15 | 65 | GND |
| B_URDY | 16 | 66 | B_DVRDY |
| B_08 | 17 | 67 | B_00 |
| B_09 | 18 | 68 | B_01 |
| B_10 | 19 | 69 | B_02 |
| B_11 | 20 | 70 | B_03 |
| B_12 | 21 | 71 | B_04 |
| B_13 | 22 | 72 | B_05 |
| B_14 | 23 | 73 | B_06 |
| B_15 | 24 | 74 | B_07 |
| GND | 25 | 75 | GND |
| C_URPLY | 26 | 76 | C_DVRPLY |
| GND | 27 | 77 | GND |
| C_URDY | 28 | 78 | C_DVRDY |
| C_08 | 29 | 79 | C_00 |
| C_09 | 30 | 80 | C_01 |
| C_10 | 31 | 81 | C_02 |
| C_11 | 32 | 82 | C_03 |
| C_12 | 33 | 83 | C_04 |
| C_13 | 34 | 84 | C_05 |
| C_14 | 35 | 85 | C_06 |
| C_15 | 36 | 86 | C_07 |
| GND | 37 | 87 | GND |
| D_URPLY | 38 | 88 | D_DVRPLY |
| GND | 39 | 89 | GND |
| D_URDY | 40 | 90 | D_DVRDY |
| D_08 | 41 | 91 | D_00 |
| D_09 | 42 | 92 | D_01 |
| D_10 | 43 | 93 | D_02 |
| D_11 | 44 | 94 | D_03 |
| D_12 | 45 | 95 | D_04 |
| D_13 | 46 | 96 | D_05 |
| D_14 | 47 | 97 | D_06 |
| D_15 | 48 | 98 | D_07 |
| SPARE (TP33) | 49 | 99 | SPARE (TP10) |
| SPARE (TP11) | 50 | 100 | SPARE (TP12) |

Table C-1: DCE-1400 to CPX-1403 Interconnect Cable Pin Assignments

# Appendix C
# Reference Map of Control Registers



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